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III-V MOSFETs from Planar to 3D

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III-V MOSFETs from Planar to 3D

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To Sheng

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III-V MOSFETs from Planar to 3D

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Si complementary metal-oxide-semiconductor (CMOS) technology has been prospered through continuously scaling of its feature size. As scaling is approaching its physical limitations, new materials and device structures are expected. High electron mobility III-V materials are attractive as alternative channel materials for future post-Si CMOS applications due to their outstanding transport property. High-k dielectrics/metal gate stack was applied to reduced gate leakage current and thus lower the power dissipation. Combining their benefits, great efforts have been devoted to explore III-V/high-k/metal metal-oxide-semiconductor field-effect-transistors (MOSFETs). The main challenges for III-V MOSFETs include interface issues of high-k/III-V, source and drain contact, silicon integration and reliability.

A comprehensive study on III-V MOSFETs has been presented here focusing on three areas: 1) III-V/high-k/metal gate stack: material and electrical properties of various high-k dielectrics on III-V substrates have been systematically examined; 2) device architecture: device structures from planar surface channel MOSFETs and buried channel quantum well FETs (QWFETs) to 3D gate-wrapped-around FETs (GWAFETs) and tunneling FETs (TFETs) have been designed and analyzed; 3) fabrication process: process flow has been set up and optimized to build scaled planar and 3D devices with feature size down to 40nm.

Potential of high performances have been demonstrated using novel III-V/high-k devices. Effective channel mobility was significantly improved by applying buried channel QWFET structure. Short channel effect control for sub-100nm devices was enhanced by shrinking gate dielectrics, reducing channel thickness and moving from 2D planar to 3D GWAFET structure. InGaAs TFETs have also been developed for ultra-low power application. This research work demonstrates that III-V/high-k/metal MOSFETs with superior device performances are promising candidates for future ultimately scaled logic devices.

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Chapter 1: Introduction

1.1 History of Scaling

Semiconductor industry has advanced itself by continuously and rapidly improving its products: electronics that used in computing infrastructures, mobile devices, automatics, medical devices and many more. In the past five decades, development of this industry profoundly changes the way people live and think. Semiconductor industry provides information and technology that generate as much as 10 percent of global gross domestic products [1]. The success of semiconductor industry can be attributed to two driving forces: 1) economic drive – the need to lower the cost. Research results are closely bound to products. They are paid by customers rather than government. Lowering the cost becomes the major measure of competition between semiconductor companies; 2) social drive – the need to improve the performance. Desires to advance communication and transport, to improve health care and security, and to save energy all request breakthrough of technology limitations. Fortunately, for semiconductor industry, these two needs are answered simultaneously by reducing the feature size of its fundamental building block – MOSFET.

MOSFET stands for metal-oxide-semiconductor field-effect-transistor. It works as a switch, which can conduct or block current depending on the voltage control. By reducing the size of MOSFETs, chip size is smaller. The more chips fit into one wafer, the less it costs for making each chip:

$$Chip\ cost = \frac{Wafer\ cost}{(No.of\ Chip\ per\ wafer\ \times Chip\ yield)} \quad (1.1)$$

On the other hand as the feature size of MOSFET shrink, it can turn on and off faster. According to Dennard's scaling theory [2], by proportionally reducing device' s structural parameters, device's characteristics improve accordingly as shown in table 1.1.

In this way, all the electrical fields in the scaled transistor remain the same. With dimensions reduce k, the power delay product reduce ~k^3.

Table 1.1. Dennard's scaling theory [2]

Parameters	Scaling
Dimensions	$x', d'_{ox}, x'_j \rightarrow x/k$
Voltage	$V' \rightarrow V/k$
Doping	$N'_{sub} = N_{sub} \cdot k$
Current	$I'_D = \mu_{eff} \frac{W}{L} \frac{\varepsilon_{ox}}{t_{ox}/k} \frac{(V_g - V_{th})^2}{2k^2} \rightarrow I_D/k$
Power	$P' = I'V' \rightarrow P/k^2$
Power Delay Product	$P't' \rightarrow Pt/k^3$

Based on all these good reasons to scale, the feature size of MOSFET has decreased ~X400 since 1970 [3]. Figure 1.1 illustrates the trend of minimum feature size and transistor density in microprocessor from 1970 to recent [4]. As the famous Moore's law predicted, or rather under the control of Moore's law, the density of transistors per chip doubled every two years [5]. Before 130nm technology node, it is the ideal scaling phase, where everything scales and performance improvement is concomitant. However, going down to 90nm and 65nm technology node, oxide couldn't be further reduced since there were only 4 atomic layers left [6][7]. Gate leakage could be huge due to the tunneling current through this thin oxide. Strained silicon technology was then introduced to enhance mobility and keep the momentum of performance improvement [8]. At 45nm technology node high-k/metal gate was developed, which replaced the silicon oxide and poly silicon gate stack [9]. As explained in the following equations, there are two ways to improve the gate control (or increase the gate capacitance): one is to reduce T_{ox}, the other is to increase k. By applying high-k dielectrics, equivalent oxide thickness (EOT) can be

reduced without thinning down the physical thickness of gate dielectrics. Thus gate leakage remains low.

$$C = \frac{Ak\epsilon_0}{t_{ox}} \quad (1.2)$$

$$EOT = k_{SiO_2} \cdot \frac{t_{SiO_2}}{k_{high-k}} \quad (1.3)$$

At 22nm node FinFETs have been pioneered [10-12]. With multi-gated structure, intel's 22nm FinFET has been reported to make chips run as much as 37 percent faster and it would be able to cut power consumption as much as 50 percent [13]. MOSFETs' performance for Intel 22nm multi-gated NFETs and PFETs are illustrated in Figure 1.2.

Scaling rules have been continuously providing effective guide for CMOS technology to satisfy two requirements stated in the beginning: scale-up circuit by increasing transistor density; and compute faster by improving switch performance.

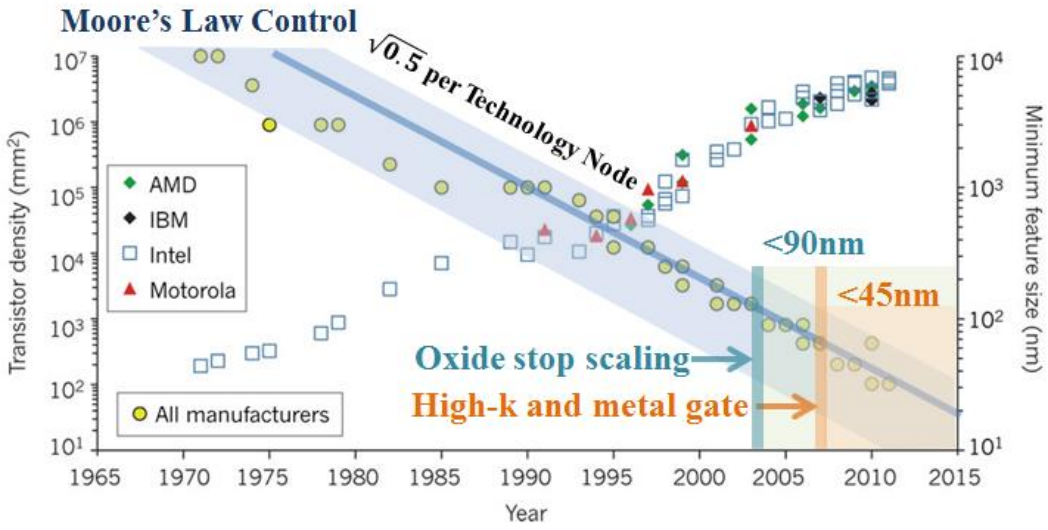


Figure1.1 The evolution of transistor gate length (minimum feature size) and the density of transistors in microprocessors over time [4]

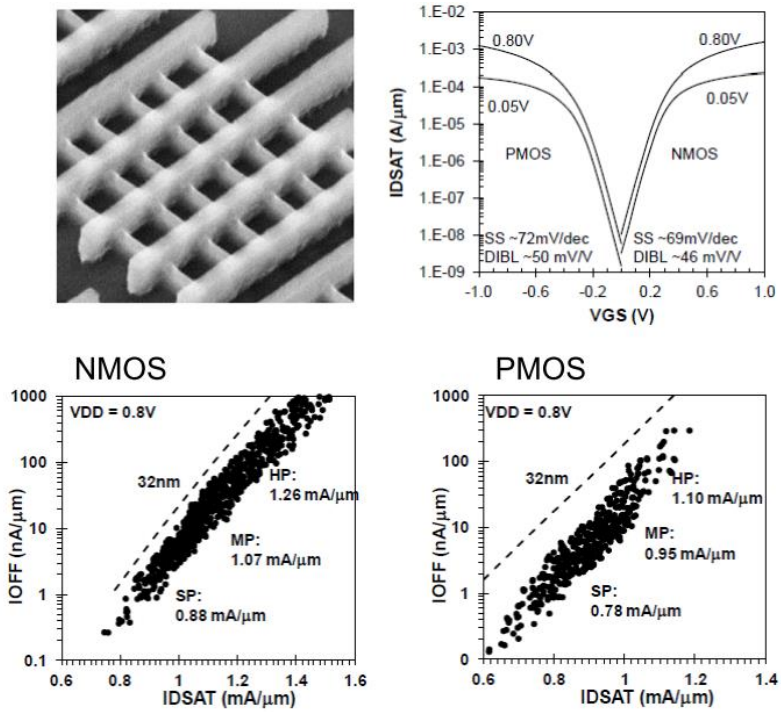


Figure1.2 Device performance of Intel 22nm multi-gated MOSFETs for both NFETs and PFETs [10]

1.2 EVOLUTION OF MOSFETS

In order to keep pace with requirements for cost and performance, MOSFETs have been evolved in many aspects including material, process flow and device structures. Silicon MOSFETs were invented in around 1960 as a three terminal controller with source, drain and gate [14]. Source and drain are formed by opposite doping to substrate. Gate controls channel by electrical field that penetrating the gate dielectric. Many techniques have been developed to enable scaling and performance improvement since then. Self-aligned process was developed around 1970 where the gate length is at around 2um. This technique largely reduced the overlap between gate and n+ region results in a much smaller parasitic capacitance. In 1980, as the gate length scaled down to

less than 1um, hot electron effect becomes a severe phenomenon which limited further gate length reduction [15][16]. Hot electrons are electrons that accelerated by the high drain voltage and become energetic when traveling through source to drain. As electrons gain enough energy, they attempt to jump into the gate dielectric which leads to damage of oxide and increase of gate leakage current. Lightly doped drain (LDD) device was then invented to reduce electric field at drain side by extending a lightly doped region at source and drain [17]. Around 1990, silicide self-aligned technique was developed to reduce the parasitic resistance at source and drain [18]. During the same time, pocket or halo implantation was also added to ease the short channel effect [19][20]. In general, during scaling of bulk devices, short channel effect was handled by two methods: 1) shrinking EOT; 2) reducing depletion layer thickness. However, as the gate length went down to a couple of hundred of nanometer, short channel effect including threshold voltage decreasing, source and drain pinch off, drain induced barrier lowering (DIBL) and subthreshold slope degradation became more and more difficult to subside [21].

Further scaling of bulk device requires very high body doping to reduce depletion layer thickness. This would lead to a higher threshold voltage. The fundamental issue that underlies bulk MOSFETs is that there is too much silicon for gate to control. Silicon on insulator (SOI) structure was invented and put into production near year 2000 to cut off the leakage path underneath [22][23]. With a buried oxide, the depletion layer thickness is defined by the thin silicon layer on top of the box oxide. Short channel control is significantly improved and junction capacitance is reduced. The major problems come along with SOI include threshold voltage variation, floating body effect and increased thermal resistance.

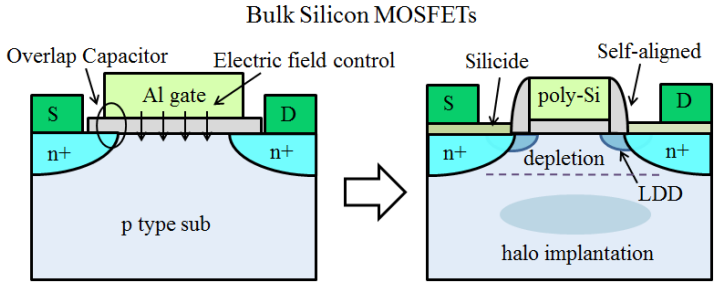


Figure1.3 Evolution of silicon bulk device

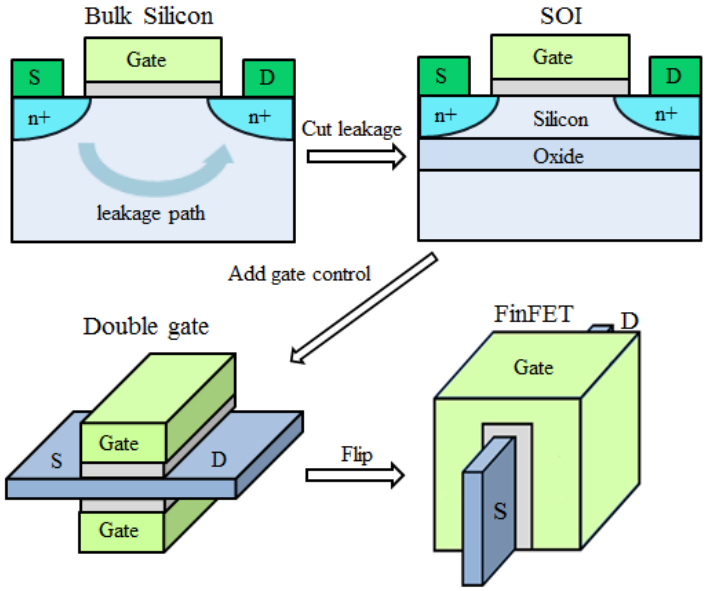


Figure1.4 Evolution of MOSFETs structure – from planner to 3D multi-gate FET

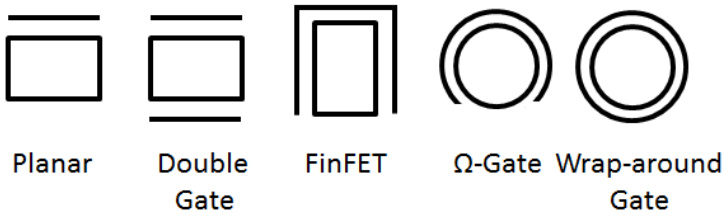


Figure1.5 Simplified gate evolution pattern

Double gate structure was developed based on SOI by changing the box oxide substrate to a second gate [24]. Having two gate controlling channel, short channel effect can be further limited [25]. FinFET structure came out by standing up the double gate devices [26]. Besides benefit of the short channel control benefit, tri-gate MOSFETs or FinFETs also offer higher drive current per area. The challenges for FinFETs mostly lie in fabrication difficulties such as fin thickness variation, doping variation and metal gate work function control.

1.3 NOVEL DEVICE ARCHITECTURE – NANOWIRE AND TFETS

As the device dimension entered the 7nm and 5nm node, it would be difficult or if not impossible to operate the transistor using MOS device physic as the basic principle. Several challenges are posted on 2012 ITRS including implementation of multi-gate structures, controlling source/drain series resistance, further scaling of EOT with higher k materials, threshold voltage control with metal gate stack [27]. The major concern for future scaling is reduction of power consumption – both on-state supply power and off-state standby power [28]. Novel device structures are expected.

To reduce the off-state power, that it, to limit the off-state leakage current, gate-wrap-around (GWA) FETs or nanowire devices currently attract lots of attentions [29-34]. GWAFETs are often considered as a quasi-1D device similar to nanowire structure with channel surrounded by dielectric and metal. By applying gate wrapped around structures, the advantage of electrostatic control can be maximized. Also, as short channel effect is much better controlled by gate, the doping concentration in channel doesn't need to be that heavy. Intrinsic channel could be applied which will largely eliminate doping number variation issue. In addition, nanowire structure has higher

integration density that nanowires can be stacked 3D both vertically or laterally (Figure 1.6). Cost-effective bottom-up fabrication solution is another merit of nanowire devices. However, several challenges remain: in fabrication, variation in nanowire diameter lead to the variation of threshold voltage; the off-state leakage current is dominated by the worst one of the nanowire in a bunch of nanowires; in device physics, due to the small size of the nanowire, strong quantum effect pushes electrons from surface inversion to bulk inversion (or volume inversion). This will reduce the carrier concentration in channel and thus decrease drive current.

Reduction of the on-state power consumption requests a lower supply voltage. For conventional MOSFETs, to reduce the supply voltage and maintain performance would mean scaling the threshold voltage and therefore increase the off current, and standby power consumption goes up accordingly. This is because conventional MOSFETs are limited to a subthreshold swing of 60mV/dec at room temperature (Figure 1.7). The basic operation mechanism of MOSFETs is to inject carriers over the potential barrier between source and channel. The height of this barrier is controlled by gate voltage. Drain current can be written as:

$$I_D \propto \exp\left(\frac{\mathrm{qV}}{\mathrm{kT}}\right) \quad (1.4)$$

$$\mathrm{SS} = \ln 10 \cdot \frac{dV_{GS}}{dI_D} \quad (1.5)$$

Thus, SS is limited to $\mathrm{kT/q}$, at room temperature, it is 60mV/dec.

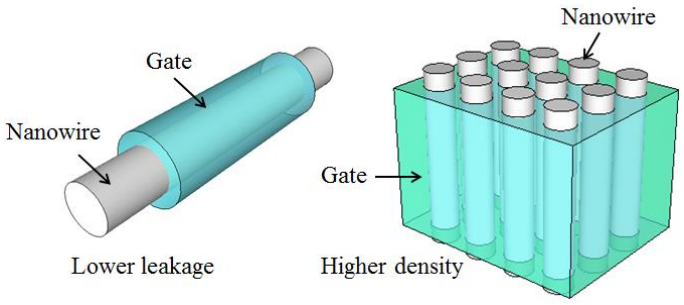


Figure1.6 Advantages of nanowire transistors

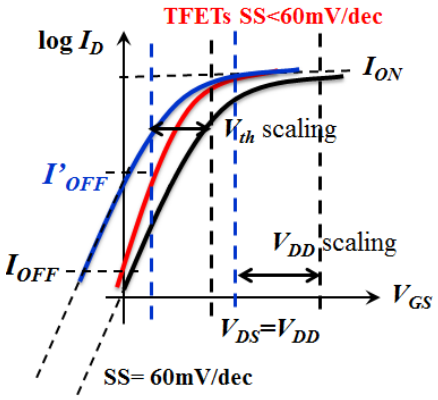


Figure1.7 Advantages of tunneling FETs over conventional MOSFETs

Tunneling FET (TFET) using different operation principle is an attractive alternative for low power application because of its potential to achieve SS < 60 mV/dec [35-39]. In TFETs, instead of moving above the potential barrier, carriers tunnel through the barrier of source and channel. In this way, the drive current is presented as:

$$I_D = a \cdot V_{eff} \cdot E \cdot \exp\left(-\frac{b}{E}\right) \quad (1.6)$$

where V_{eff} is tunnel junction bias; E is electric field; a,b are coefficients determine by material's band gap E_g and effective mess m*.

$$SS = \ln 10 \cdot \left[\frac{1}{V_{eff}} + \frac{(E + b)}{E^2} \cdot \frac{dE}{dV_{eff}}\right]^{-1} \quad (1.7)$$

SS depends on electrical field and effective voltage, not limited by kT/q [40].

To achieve a lower SS using TFET structure: 1) junction need to be highly doped and kept as sharp as possible to maximize dE/dV; 2) gate voltage should be effectively coupled to tunneling junction bias V_{eff}. The drive current of TFETs can be improved by increase V_{eff}, E, decrease E_g and effective mess m*.

1.4 Emerging Channel Material – III-V Compound

III-V materials are compounds that formed with elements from group III such as Al, Ga, In and elements from group V like N, P, As, Sb. III-V materials are by no means new to semiconductor industry. Researchers have been considering III-V as the substrate material since the invention of MOSFETs and the first demonstration of depletion mode GaAs MOSFETs was around four decades ago. III-V materials are also widely used in optical applications. One famous example would be GaN blue light emitting diode (LED). Different than silicon, III-V materials are direct band materials with smaller band gaps, as illustrated in Figure 1.8 [41]. III-V has been recognized as alternate channel material due to their outstanding transport advantages. In explicit, that is their lower effective mess and higher mobility [42][43]. When transistor first developed, electrons run in vacuum as the name "vacuum tube" indicated. Then transistors on silicon were invented. With electrons travel in silicon crystal, the effective mess dropped to $0.26m_0$. III-V materials inherently process an even lower effective mess, for example the effective mess of InGaAs is $0.04m_0$. Recently great efforts have also been allocated into graphene where the effective mess is close to 0. The trend is clear, lower effective mess, faster the transport (Figure 1.9). The related material properties of Si, Ge and main III-V for MOSFETs application are shown in Table 1.2. With superior mobility, III-V materials can potentially provide higher drive current.

$$I_D = Cox \cdot \mu \frac{W}{L} \frac{(V_g - V_{th})^2}{2} \quad (1.8)$$

Or enable lower supply voltage to achieve the same current level (Figure 1.10). With various choices of group III-V compound semiconductors, it is possible to continuously change the band gap and lattice constant by forming alloys of different III-Vs, which largely broaden the design of the device structure.

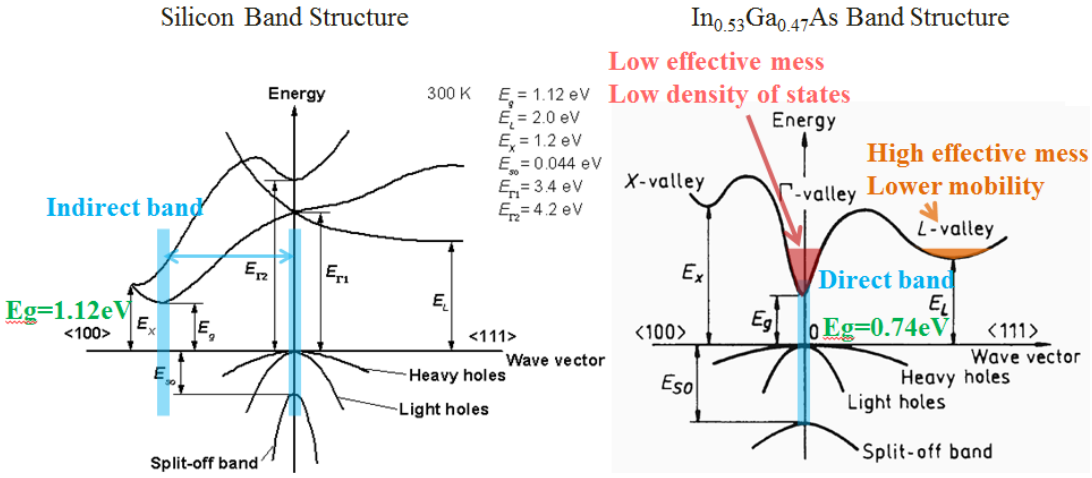


Figure1.8 Band structures of silicon and InGaAs

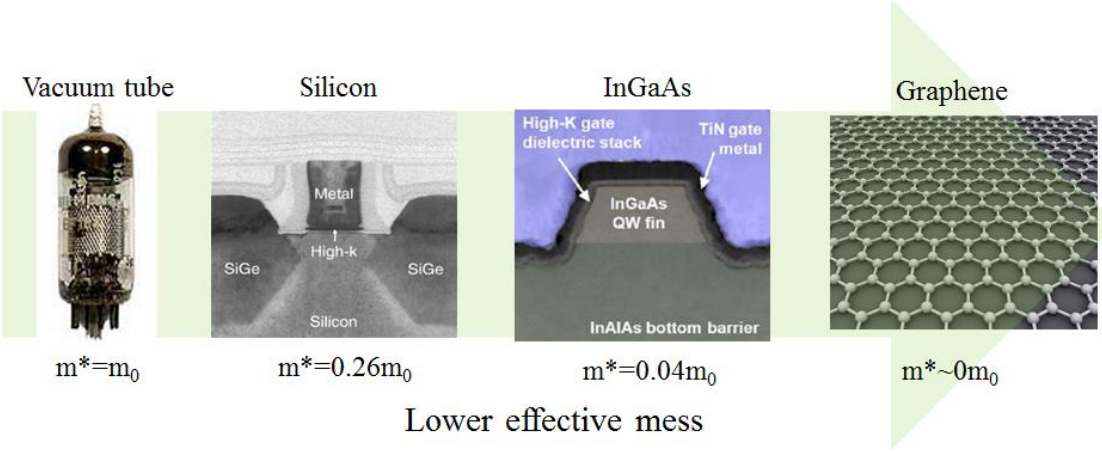


Figure1.9 Trend of new materials: lower effective mess.

Table 1.1 Related material properties of Si, Ge and main III-V for MOSFETs application

	Si	Ge	GaAs	InP	$In_{0.53}Ga_{0.47}As$	$In_{0.7}Ga_{0.3}As$	InAs
Lattice constant (Å)	5.431	5.658	5.653	5.869	5.869	5.937	6.058
Electron Effective Mass (m^*/m_0)	0.19	0.082	0.067	0.077	0.041	0.034	0.023
Electron Affinity (eV)	4.05	4	4.07	4.38	4.5	4.65	4.9
Band-gap (eV)	1.12	0.66	1.42	1.35	0.74	0.58	0.35
Electron Mobility (cm^2/Vs)	1,500	3,900	8,500	4,600	12,000	20,000	33,000
Hole mobility (cm^2/Vs)	450	1,900	400	150	300	400	460

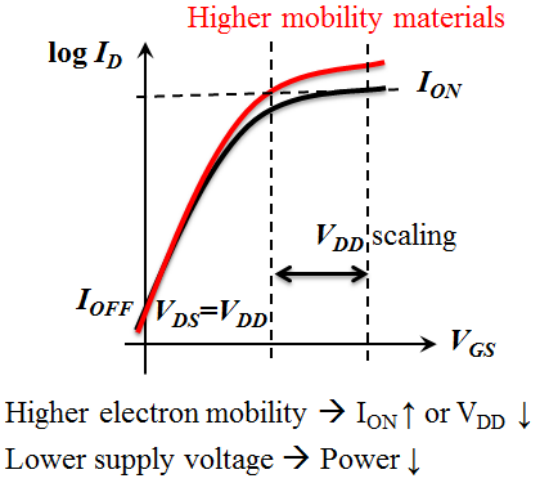


Figure1.10 Transfer characteristics of MOSFETs to illustrate the advantage of higher mobility materials.

When III-V MOSFETs first developed, the major issue was lack of high quality thermodynamic stable gate dielectrics. Unlike Si-SiO_2 interface, the native oxides of III-V produce much more interface traps, which makes it difficult to band Fermi level into inversion mode. Namely "the Fermi level pinning issue" [44-46]. Significant progresses have been made in the past two decades in solving these problems and essentially enable III-V material to outperform Silicon. Atomic layer deposition (ALD) has been introduced

to III-V MOSFETs to apply high-k dielectrics such as Al_2O_3, HfO_2, ZrO_2 or $LaAlO_3$ with a reasonable interface trap density (D_{it}) [47-50]. Molecular beam epitaxial (MEB) $Ga_2O_3(Gd_2O_3)$ dielectrics has been reported to show good interface quality with D_{it} at mid-$10^{11}/cm^2 \cdot eV$ level [51-53]. A variety of surface treatment techniques have also been explored for III-V surface, such as using chemicals like sulfur [54], HBr [55], and oxy-nitride [56], fluorine plasma [57][58], and Si, Ge, Si_xN_y, Ge_xN_y interfacial passivation layers [59-62] . All of these methods have shown promising improvement of device performance.

The following challenges exist for developing III-V MOSFETs: 1) Gate stack: further scaling of EOT with higher k materials is needed. High-k/III-V interface trap need to be better controlled. However, note that as the gate dielectric thickness continues to reduce, the gate capacitance will keep increasing and interface trap capacitor will no longer be a dominant issue. 2) Source and drain resistance: as the channel goes shorter and shorter, series resistances at source and drain become a limiting factor of current capacity. Self-aligned process similar to silicide technique is still under searching. 3) Integration on silicon: III-V materials have poor mechanical properties and for industry application concerns, integrate III-V on silicon substrate is necessary. Also, III-V are superior for electron mobility but not for hole mobility. Integration of Ge pFETs and III-V nFETs on silicon substrate would be an ideal solution to boost the CMOS performance. 4) Process complexity: to suppress the off-state leakage current, multi-gated channel shape or nanowire structure is in demand. Basic process issues same as silicon 3D multi-gated devices need to be addressed.

When designing a III-V MOSFET, several points need to be bear on mind on the intrinsic limitations of III-V MOSFETs: 1) Low conduction band density of states: lower effective mess for III-V materials come from the curvature of their conduction band

(Figure 1.8). With this shape of conduction band, however, density of states is also lower. The current flow is a product of mobility and concentration of electrons. For III-V materials, the current enhancement resulted from higher mobility is compromised by the lower conduction band density of states. As the dielectric scaling down further, the surface carrier concentration tends to become a dominant factor which might cancel out the benefit from higher mobility. 2) Band to band tunneling: when smaller effective mess materials are selected for higher mobility, the band gap drops accordingly. For example, the high mobility material InSb has band gap of only 0.17eV. With smaller band gap, the band to band tunneling can be a limiting factor for off-state leakage current. 3) Ballistic transport regime: ballistic transport means that the channel is so short that electrons travel from source to drain without encountering any scattering. From ballistic theory, the on current is determined by the number of carriers flow through the channel per unit time rather than by channel mobility. We can still present the current using the mobility concept:

$$I_D = \frac{W}{L_g}\mu_{app}C_G(V_{GS} - V_T)V_{DS} \quad (1.9)$$

$$\frac{1}{\mu_{app}} = \frac{1}{\mu_B} + \frac{1}{\mu_0} \quad (1.10)$$

The apparent channel mobility μ_{app} is the combination of the ballistic mobility μ_B and the bulk mobility μ_0 using Mathiessen's law [63]. In this way, the apparent mobility can be explained in both ballistic and diffusion limit. When the gate length goes down into ballistic region, μ_{app} will become more and more dominate by μ_B not μ_0 and III-V is losing its advantage. 4) Transfer to lower mobility valley: as indicate in Figure 1.8, the conduction band of III-V has multiple valleys Γ, L and X with different effective mess. When apply the gate electric field, the electrons fill up the Γ valley first since it is the lowest valley. As gate voltage keep cranking up, electrons tend to move to

the L valley as well where effective mess increases and mobility drops [63]. When design the III-V alloy, it is preferred to have larger energy level difference between different valleys.

1.5 OUTLINE

This research work aims at exploring the possibility of III-V compound as alternative channel material and developing emerging device architectures for next generation CMOS technology. III-V materials are selected here for their high electron mobility and thus the potential to achieve higher drive current. This research work started from designing the gate stack using various high-k dielectrics/metal gate and went on to surface channel MOSFETs demonstration. Then the study of buried channel MOSFETs with a thin barrier layer applied on top of the channel were carried out to further improve the effective channel mobility. 3D gate-wrapped-around FETs were investigated after to optimize the gate control over channel. III-V tunneling FETs with a novel device operation concept have also been examined. Research efforts have been devoted into many areas to improve the III-V device performance including high-k/metal gate stack quality, high-k/III-V interface properties, channel layer quantum well structure design, source/drain contact and fabrication process flow.

In chapter 2, high-k/metal gate stack applied on InGaAs substrate was investigated. MOSCAPs were fabricated with various high-k dielectrics using atomic-layer deposition. Interface property of high-k/InGaAs and metal gate work function was studied. Surface channel InGaAs MOSFETs with ALD high-k dielectrics deposited directly on top of the channel have been fabricated. Device performances including drive current, transconductance, subthreshold swing and effective channel mobility of devices

with various high-k dielectrics have been compared. Effect of Indium concentration dependence in InGaAs channel has also been examined.

In chapter 3, to further improve the effective channel mobility for III-V MOSFETs, buried channel structure has been applied. InGaAs buried channel MOSFETs with various barrier layers were studied. By applying a thin barrier layer between channel and high-k dielectric, the problematic high-k/III-V interface is moved away from the channel and thus the interface scattering is significantly reduced. Scaling behaviors of InGaAs MOSFETs down to gate length of 40nm has been investigated including V_{th} roll-off, SS and DIBL. Channel thickness of InGaAs has been thinning down to achieve better short channel effect control. Higher mobility material InAs has also been inserted into InGaAs channel to achieve better on-state performance.

In chapter 4, non-planar gate-wrapped-around structure has been applied to III-V InGaAs MOSFETs. 3D InGaAs GWAFETs with ALD high-k dielectrics have been fabricated with various fin width down to 40nm. InGaAs/InP heterostructure was applied to enable fin release process. Optimized fabrication process flow has been set up. Scalability of 3D devices has been studied and compared to planar devices including drive current, transconductance, SS, DIBL and off-state leakage. Simulation using Sentaurus of 3D InGaAs nanowire structure has been carried out to better understand the performance limiting factors.

In chapter 5, InGaAs tunneling FETs have been demonstrated. Band to band tunneling operation mechanism was confirmed by the gate bias dependent Esaki diode behavior. InGaAs TFETs have been fabricated using MBE grown tunneling junctions. Device performances of TFETs with p++/i and p++/n+ junction and different high-k dielectrics have been compared.

In chapter 6, the contribution of this dissertation is summarized and suggestions on future work have been proposed.

Chapter 2: Surface Channel InGaAs MOSFETs

As significant efforts have been devoted to explore III-V materials recently [64], encouraging results have been reported that III-V MOSFETs with various high-k dielectrics Al_2O_3, HfO_2 and ZrO_2, molecular beam epitaxy (MBE) Ga_2O_3 (Gd_2O_3) dielectrics and Si interfacial passivation layer (IPL) all show promising performance improvement. $In_{0.53}Ga_{0.47}As$ surface channel MOSFETs with ALD high-k dielectrics were studied here. Within various III-V compound materials, InGaAs/InAlAs system is preferred because of several reasons: 1) the electron mobility of InGaAs is comparably high. $In_{0.53}Ga_{0.47}As$ exhibits intrinsic electron mobility of 12,000cm^2/eVs at room temperature; 2) Band-to-band tunneling leakage current is limited since the band gap for $In_{0.53}Ga_{0.47}As$ is around 0.74eV. Off-state leakage current for InGaAs devices is lower than smaller bandgap materials like InAs and InSb; 3) InGaAs/InAlAs is lattice matched and can be grown by MBE techniques with low defect density.

High-k dielectrics deposited using atomic layer deposition were applied here because of their advantages on higher film uniformity, accurate control of dielectric thickness and better interface condition due to self-cleaning characteristics. In this chapter, the following topics will be covered: 1) Material and electrical properties of various high-k and metal gate stack including the interface and bulk property of high-k layer, leakage current and metal gate work function; 2) detailed fabrication process for surface channel InGaAs MOSFETs; 3) Comparison of InGaAs MOSFETs with Al_2O_3 and ZrO_2 dielectrics; 3) Effect of Indium concentration dependence on device performance of InGaAs surface channel MOSFETs.

2.1. DESIGN OF HIGH-K/ METAL GATE STACK

High-k/metal gate stack was adapted into semiconductor industry at 45nm technology node and beyond to enable further scaling of gate dielectrics. When select a gate dielectric, several factors need to be considered: 1) larger band gap is preferred. The conduction band and valance band offset to the substrate material also need to be examined. Barrier height should be large enough for both electrons and holes to prevent leakage; 2) this dielectric should process a good interface with substrate material with low interface trap density; 3) the bulk property of oxide is also important. Low fixed charge and traps are preferred; 4) it should be thermal dynamically stable during the fabrication process; 5) it need to be compatible to gate electrode [65-67].

Atomic layer deposition was introduced to silicon-based CMOS manufacturing for its great potential on producing very thin, conformal films with accurate control of film thickness and composition at atomic level [68]. Similar to chemical vapor deposition techniques (CVD), ALD is also based on chemical reaction but limited by surface. ALD process breaks down the chemical reaction into two half reactions, by purging two chemicals (or precursors) one at a time, the film can be deposited in a self-limiting manner. ALD is done by cycles. The substrate is exposed alternatively to each precursor for a certain time. In etch cycle one layer of film at around 0.1nm is deposited. The thickness of film is controlled by the number of cycles applied [69].

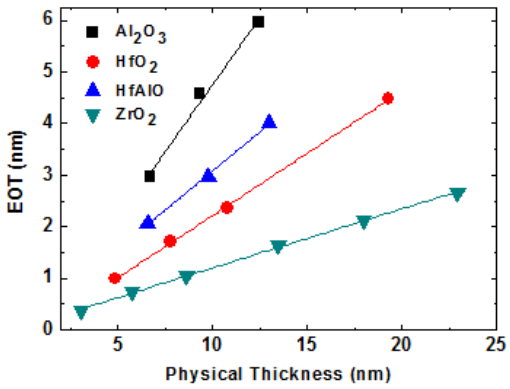
In order to understand ALD high-k dielectrics on III-V, MOSCAP of InGaAs with various high-k dielectrics have been fabricated and analyzed. The scalability of equivalent oxide thickness, high-k/III-V interface quality, oxide bulk quality were studied and compared. $In_{0.53}Ga_{0.47}As$ MOSCAPs were fabricated on 300nm MBE grown substrate by first using 1% HF to clean the InGaAs surface and remove the native oxide. Then samples were dipped into ammonium sulfur for surface passivation. The purpose of

ammonium passivation is believed to be that the dangling bonds of InGaAs surface can be terminated by sulfur, which can better protect the surface from being oxidized [70]. Samples were then transferred to ALD chamber where various thicknesses of high-k film Al_2O_3, HfO_2, ZrO_2 and HfAlO were deposited. ALD system used here is Savannah 100 Optimum. Chamber temperature is set to be 200ºC and base pressure is 0.24 mTorr. Chamber temperature and pressure need to be adjusted for different ALD system. After ALD, post deposition annealing was done using rapid thermal annealing (RTA) at 500C for 90s to densify the oxide film. TaN was sputtered as gate electrode and patterned by CF_4 reactive ion etching (RIE). The last step was backside metal deposition and annealing at 400C for 30s to form the backside contact.

Figure 2.1 illustrates the EOT vs. physical thickness for different high-k materials. k values for these materials are summarized in table aside. EOT was extracted from CV-measurement using inversion region capacitance. ZrO_2 shows the highest scalability with k value of 32. For a 5nm thick ZrO_2, EOT is scaled down to 0.7nm. Flat band voltage shift vs. EOT for Al_2O_3, HfO_2, ZrO_2 and HfAlO were plotted in Figure 2.2. Fixed charge was extracted from slope of flat band vs. EOT:

$$V_{fb} = V_g @ \min\left[\frac{d\left(\frac{1}{C}\right)}{dV}\right] \quad (2.1)$$

$$V_{fb} = \varphi_{fermi} - \left(\frac{Q_f}{\varepsilon_{OX}}\right) EOT \quad (2.2)$$



High-k material	k value
Al_2O_3	8
HfO_2	18
HfAlO	13
ZrO_2	32

Figure 2.1. EOT vs. physical thickness of ALD Al_2O_3, HfO_2, ZrO_2 and HfAlO on InGaAs substrate. k values were summarized in table.

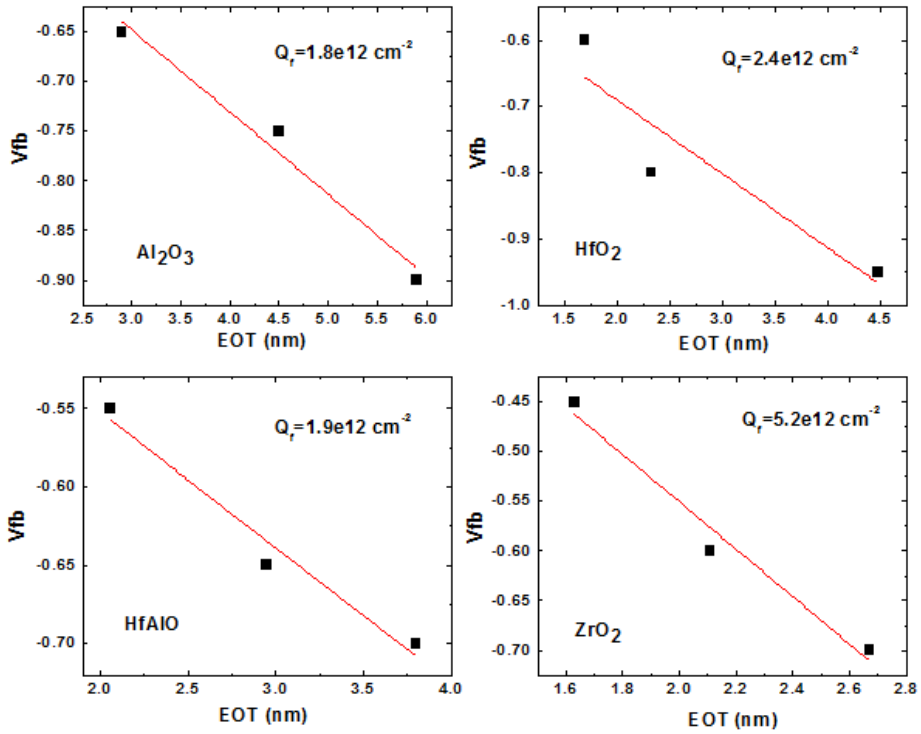


Figure 2.2. Flat band voltage shift vs. EOT for Al_2O_3, HfO_2, ZrO_2 and HfAlO on InGaAs substrate. Fixed Charge extracted from slope of the curves.

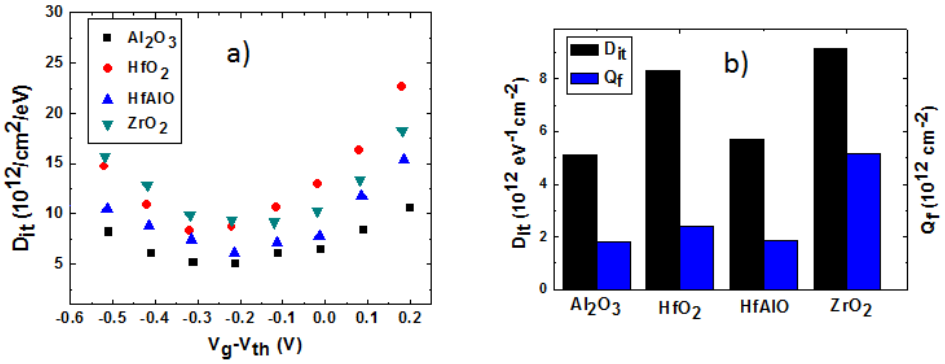


Figure 2.3. a) D_{it} measured at room temperature with frequency range from 100Hz to 1MHz for ALD Al_2O_3, HfO_2, ZrO_2 and HfAlO on InGaAs substrate. b) Comparison of D_{it} and fixed charge for ALD Al_2O_3, HfO_2, ZrO_2 and HfAlO on InGaAs substrate.

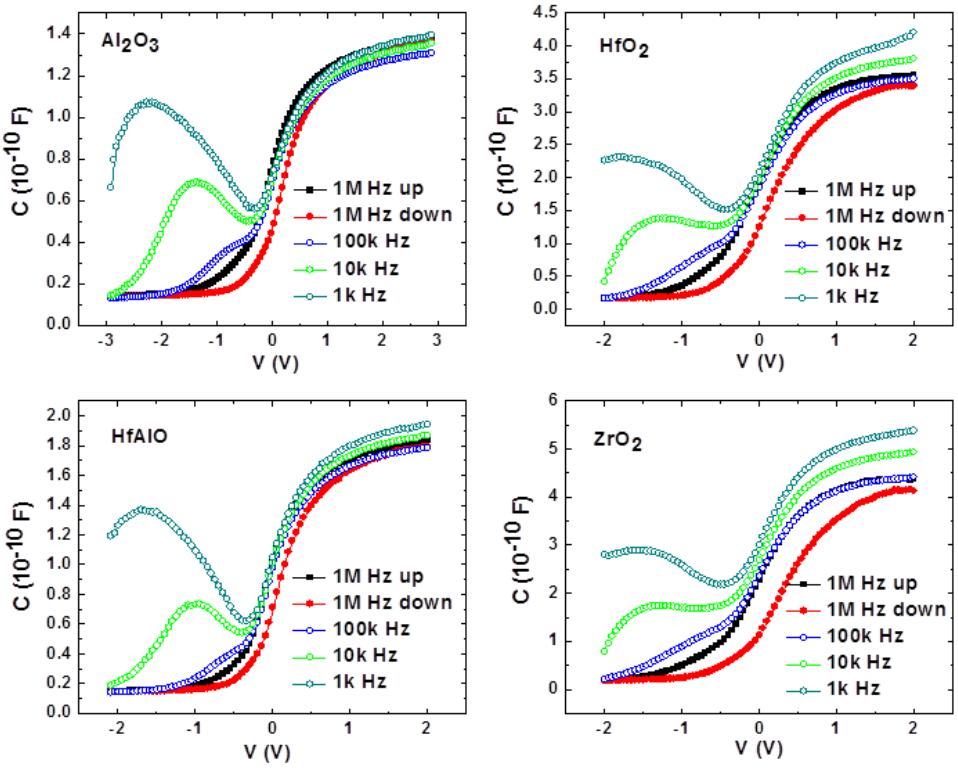


Figure 2.4. CV hysteresis and dispersion measurement of MOSCAP with ALD Al_2O_3, HfO_2, HfAlO, and ZrO_2 on InGaAs substrate at frequency from 1kHz to 1MHz.

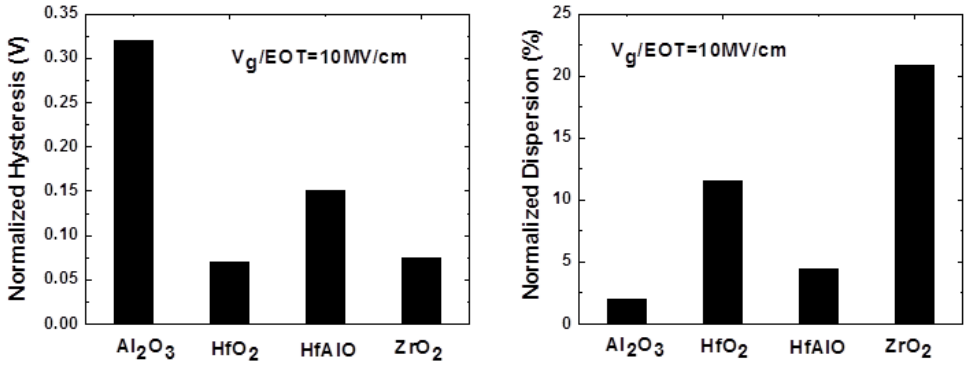


Figure 2.5. Normalized hysteresis and dispersion for MOSCAP with Al_2O_3, HfO_2, ZrO_2 and HfAlO dielectric on InGaAs substrate.

D_{it} measured by conductance method at room temperature with frequency range from 100Hz to 1MHz is shown in Figure 2.3a), with Al_2O_3 showing the lowest D_{it} of $5e^{12}$ $eV^{-1}cm^{-2}$ and ZrO2 the highest of $9e^{12}$ $eV^{-1}cm^{-2}$. D_{it} and Q_f for Al_2O_3, HfO_2, ZrO_2 and HfAlO were summarized and compared in Figure 2.3b).

Figure 2.4 illustrates the CV hysteresis and dispersion measurement of MOSCAP with different dielectrics at frequency from 1kHz to 1MHz. For fair comparison between different high-k materials, gate voltage range applied was chosen to generate same electrical field across the dielectrics. That is, the same electrical field $E = V_g/EOT = 10mV/cm$ was applied. Figure 2.5 summarized the normalized hysteresis and dispersion for Al_2O_3, HfO_2, ZrO_2 and HfAlO on InGaAs. The smallest frequency dispersion was achieved by Al_2O_3 which also indicates its better interface quality with InGaAs substrate. The results above suggest that ZrO_2 has the highest scalability however also highest interface trap density with InGaAs surface, while Al_2O_3 has a lower k value but best interface with InGaAs.

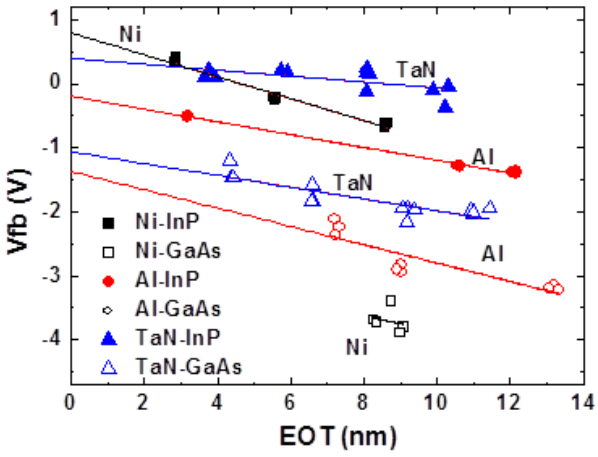


Figure 2.6. Flat band voltage vs. EOT plot for different metal gate materials: TaN, Al and Ni.

Table 2.1. Metal gate work function extracted from MOSCAP with III-V substrate and Al_2O_3 dielectrics

Metal Gate	Vacuum Metal Workfunction (eV)	Effective Workfunction on InP (eV)	Effective Workfunction on GaAs (eV)
Al	4.06 -4.26	4.19	4.13
TaN	4.5	4.78	4.43
Ni	5.04 – 5.35	5.17	--

Different metal gate materials were also applied to demonstrate Fermi-level unpinning at high-k and III-V interface. MOSCAPs were fabricated on both n type InP and p type GaAs substrate with ALD Al_2O_3 dielectric. Metal gate TaN is deposited by sputtering. Ni and Al metal gate were deposited by e-beam evaporation and lift-off process. The flat-band voltage of each sample is extracted from C-V measurement. Metal-semiconductor work function difference was shown by interpolation (Figure 2.6). Flat band voltage shifts with different metal gate materials, which indicates that Fermi-level is able to move inside the band gap.

2.2. SURFACE CHANNEL INGAAS MOSFETS WITH HIGH-K DIELECTRICS

InGaAs surface channel MOSFETs have been fabricated on MBE grown InGaAs wafer. Figure 2.7 shows the cross section of $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ MOSFET layer structures. Both samples were grown on 2-inch InP p+ substrate, followed by 100 nm, p-type doped 1×10^{18} cm^{-3} $In_{0.52}Al_{0.48}As$ buffer layer, and 400 nm p-type doped 5×10^{16} cm^{-3} $In_{0.53}Ga_{0.47}As$. For $In_{0.7}Ga_{0.3}As$ wafer, a 12 nm p-type doped 5×10^{16} cm^{-3} $In_{0.7}Ga_{0.3}As$ channel was grown on the top. The lattice mismatch for $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ is 1.16%. 12 nm is within the critical thickness range for $In_{0.7}Ga_{0.3}As$ epi-growth on $In_{0.53}Ga_{0.47}As$. Material properties of both $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ substrate were verified by X-ray photoelectron spectroscopy (XPS) measurement.

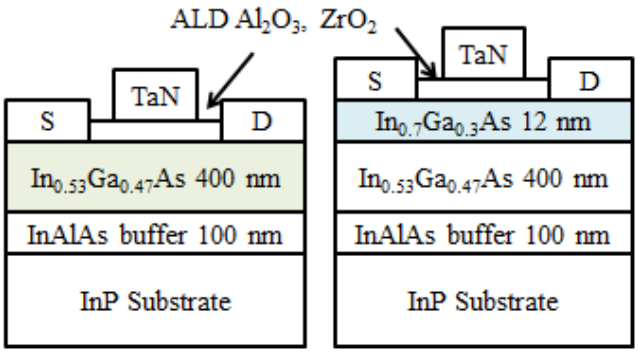


Figure 2.7. Cross-sectional schematic view of surface channel $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ MOSFETs with ALD Al_2O_3 or ZrO_2 as gate dielectric.

$In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ samples were first covered by 10 nm Al_2O_3 by ALD, which is used to protect the wafer during source and drain ion-implantation process. Dummy gate was patterned by photoresist. Source and drain was selectively doped by Si implant (dosage of 2×10^{14} cm^{-2} at 35 keV). After remove photoresist for

dummy gate, implantation activation was done by RTA at 700 ℃ 10 s in nitrogen ambient. The removal of 10 nm Al_2O_3 protecting layer was done after the dopant activation to prevent dopant from out diffusion. Samples were then cleaned using diluted HF and passivated by ammonium sulfur. Then Al_2O_3 or ZrO_2 dielectrics were grown onto both substrates by ALD. Post deposition anneal was done at 450-500 ℃ for 1 min. TaN was deposited as gate electrode by reactive sputtering. The thickness of TaN layer is around 200nm. Source and drain metal AuGe(25nm)/Ni(10nm)/Au(40nm) was defined by e-beam evaporation and lift off process, followed by 400 ℃ 30 s RTA.

I_d-V_g characteristic of $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ MOSFETs measured at room temperature (RT) and 77 K were illustrated in Figure 2.8 for a) Al_2O_3 with EOT 4.4 nm and b) ZrO_2 with EOT 0.9 nm. The gate leakage current is less than 4×10^{-9} A/cm^2 at V_g-V_{th}=1 V for Al_2O_3 samples, and 1×10^{-4} A/cm^2 for ZrO_2 samples (data not shown). For both high-k dielectrics, the $In_{0.53}Ga_{0.47}As$ MOSFETs exhibit much lower subthreshold swing than $In_{0.7}Ga_{0.3}As$ MOSFETs (125 mV/dec versus 160 mV/dec for Al_2O_3, 126 mV/dec versus 138 mV/dec for ZrO_2). This indicates a better gate control over channel due to a higher quality interface between $In_{0.53}Ga_{0.47}As$ substrate and Al_2O_3 (or ZrO_2) high-k dielectric than $In_{0.7}Ga_{0.3}As$. This is demonstrated by the interface trap density measurement. Lower D_{it} at oxide/$In_{0.53}Ga_{0.47}As$ interface was observed by conductance method (Figure 2.9). Subthreshold swing is also affected by the junction leakage current. The off current of $In_{0.7}Ga_{0.3}As$ is slightly larger due to its smaller band gap. Low temperature measurement show much lower off current due to lower generation and recombination rate at 77 K.

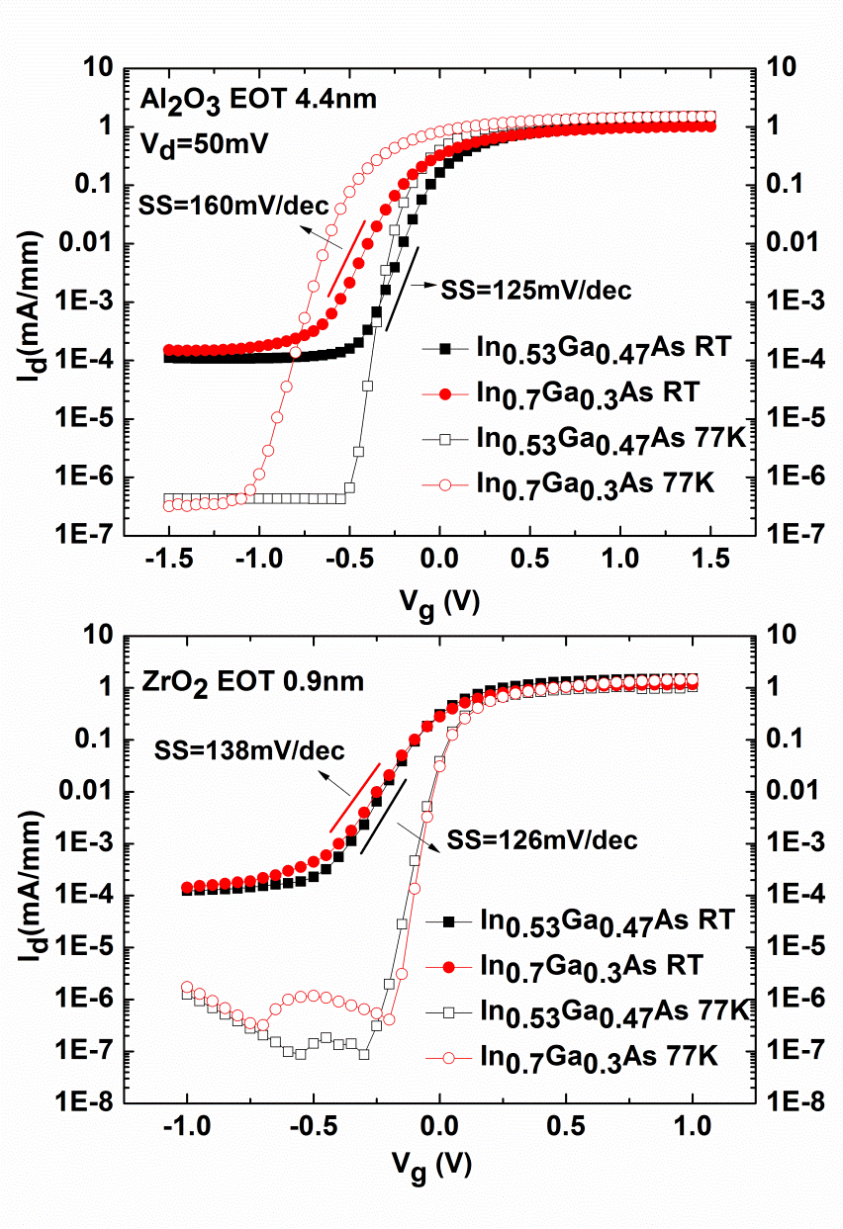


Figure 2.8. I_d-V_g characteristics at V_d=50 mV of $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ MOSFETs measured at room temperature and 77 K with a) Al_2O_3 (EOT 4.4 nm) and b) ZrO_2 (EOT 0.9 nm). L_g=20 µm.

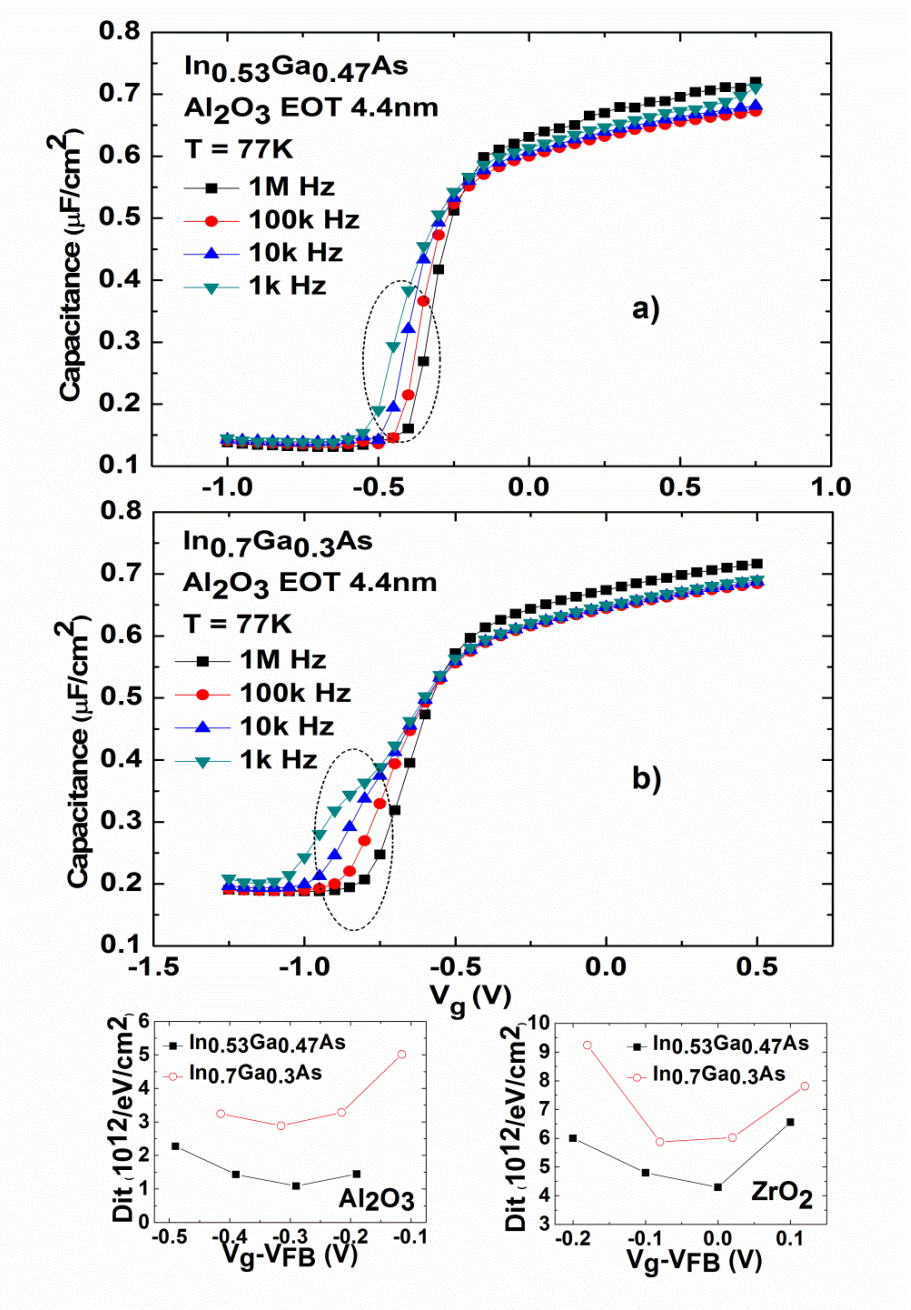


Figure 2.9. Split-CV frequency dispersion from 1 MHz to 1 KHz measured at 77 K for a) $In_{0.53}Ga_{0.47}As$ MOSFETs with Al_2O_3, b) for $In_{0.7}Ga_{0.3}As$ MOSFETs with Al_2O_3, c) D_{it} of Al_2O_3/InGaAs and d) D_{it} of ZrO_2/InGaAs.

Figure 2.9 shows split-CV of $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ MOSFETs with Al_2O_3 measured at 77 K. Frequency range is from 1 MHz to 1 KHz. Low temperature measurement was used to minimize the influence of minority carrier. Comparing to $In_{0.7}Ga_{0.3}As$ MOSFETs, the CV curves of $In_{0.53}Ga_{0.47}As$ channel MOSFETs show smaller dispersion within the depletion region (high-lighted in Figure 2.9. This suggests lower interface trap density for $In_{0.53}Ga_{0.47}As$ MOSFETs. D_{it} results are inserted in Figure 2.9. Minimal D_{it} for Al_2O_3 high-k dielectric is 1.1×10^{12} $eV^{-1}cm^{-2}$ for $In_{0.53}Ga_{0.47}As$ and 3.2×10^{12} $eV^{-1}cm^{-2}$ for $In_{0.7}Ga_{0.3}As$ MOSFETs. As for ZrO_2, $In_{0.53}Ga_{0.47}As$ MOSFETs have minimal D_{it} 4.1×10^{12} $eV^{-1}cm^{-2}$ compared to 5.8×10^{12} $eV^{-1}cm^{-2}$ for $In_{0.7}Ga_{0.3}As$ MOSFETs.

Transfer and output characteristics of $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ MOSFETs are shown in Figure 2.10. Although $In_{0.7}Ga_{0.3}As$ MOSFETs are expected to give a larger on-current and transconductance due to its higher intrinsic mobility, the results are opposite. This indicates that the III-V/high-k dielectric interface plays a more important role here. The high temperature annealing process during fabrication may also have degraded device performance.

The extrinsic transconductance and subthreshold swing of InGaAs MOSFETs with different Al_2O_3 and ZrO_2 thicknesses were summarized in Figure 2.11. At similar EOT around 2 nm, devices with Al_2O_3 show higher transconductance and smaller subthreshold swing than devices with ZrO_2. This is because the Al_2O_3 has smaller interface trap density than ZrO_2 (Figure 2.9). The advantage of ZrO_2 is that it has a higher k value (around 32) than Al_2O_3 (k=8). With same physical thickness, EOT of ZrO_2 can be

scaled even further and thus provides better gate control. However, the disadvantage is that the interface quality of ZrO_2 is worse than Al_2O_3.

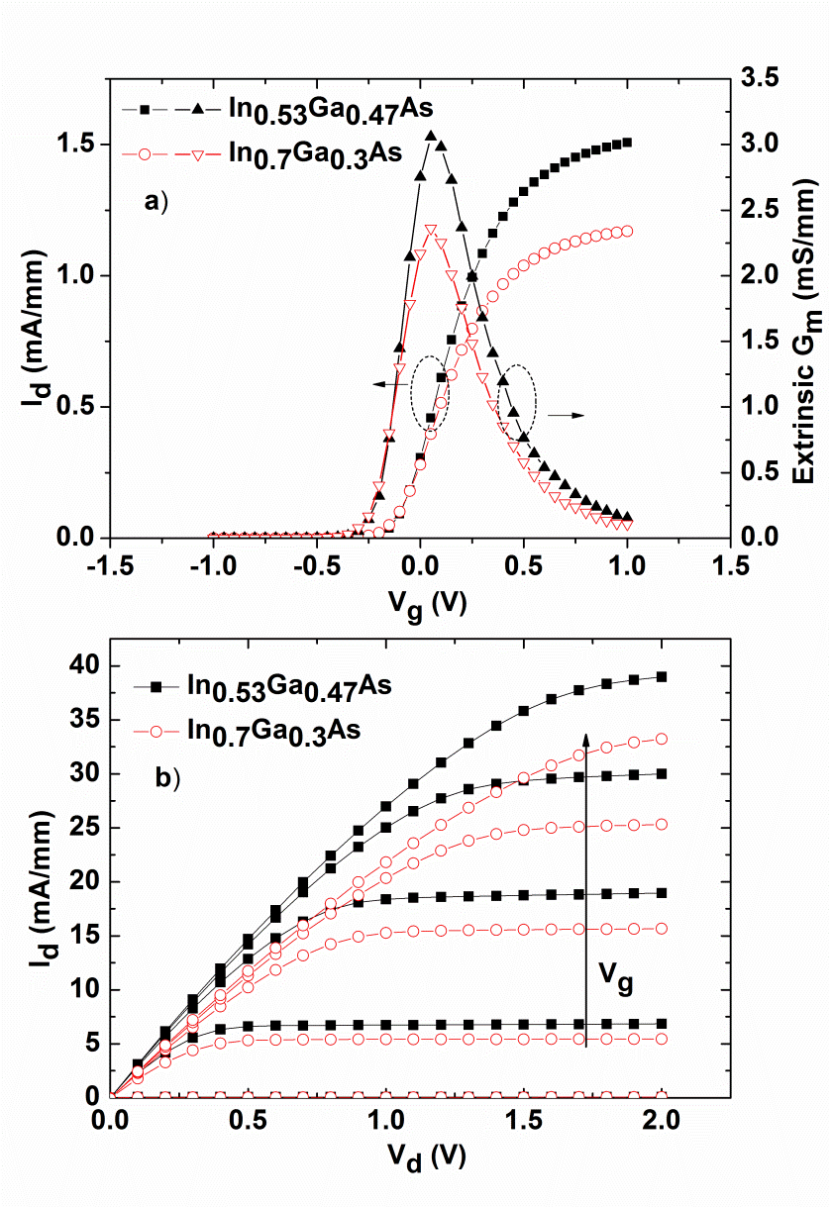


Figure 2.10. a) I_d-V_g and extrinsic transconductance G_m-V_g curves at V_d=50 mV for $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ MOSFETs with ZrO_2. b) Output characteristic of $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ MOSFETs with ZrO_2 measured from V_g-V_{th}=0 V to 2 V, at the step of 0.5 V. L_g=20 μm.

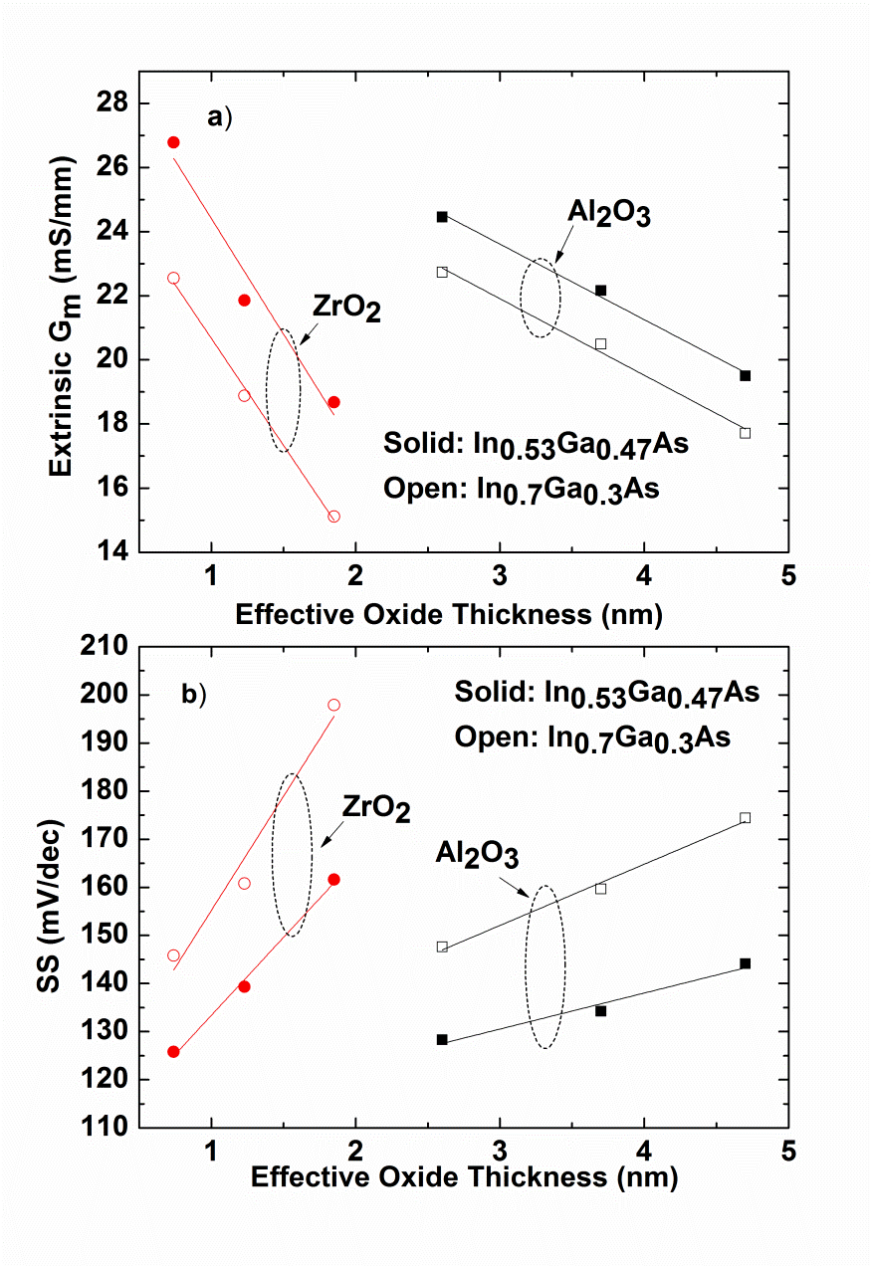


Figure 2.11. a) Extrinsic transconductance at V_d =1 V of $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ MOSFETs with various oxide thicknesses. b) Subthreshold swing at V_d =0.05 V of $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ MOSFETs with various oxide thicknesses.

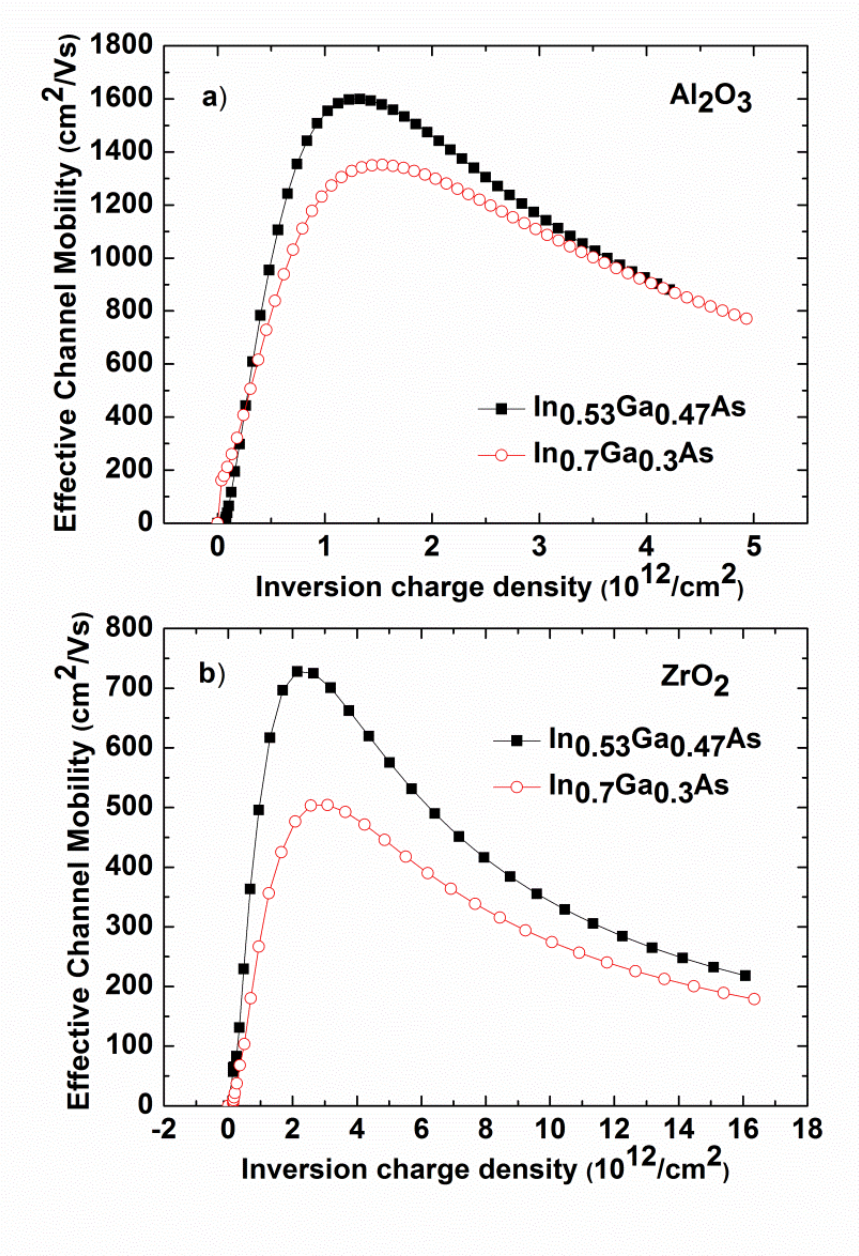


Figure 2.12. a) Effective channel mobility versus inversion charge density for $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ MOSFETs with Al_2O_3. b) Effective channel mobility versus inversion charge density for $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ MOSFETs with ZrO_2.

Effective channel mobility of $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ channel MOSFETs was measured by split-CV method. Figure 2.12 illustrates channel mobility versus inversion charge density characteristics of $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ channel MOSFETs for a) Al_2O_3 and b) ZrO_2. $In_{0.53}Ga_{0.47}As$ MOSFETs show higher mobility than $In_{0.7}Ga_{0.3}As$ MOSFETs for both gate dielectrics. The peak mobility of $In_{0.53}Ga_{0.47}As$ with Al_2O_3 (ZrO_2) is 1600 cm^2/Vs (730 cm^2/Vs), that of $In_{0.7}Ga_{0.3}As$ is 1350 cm^2/Vs (505 cm^2/Vs). These results agree with previous observation of transconductance and subthreshold swing trend.

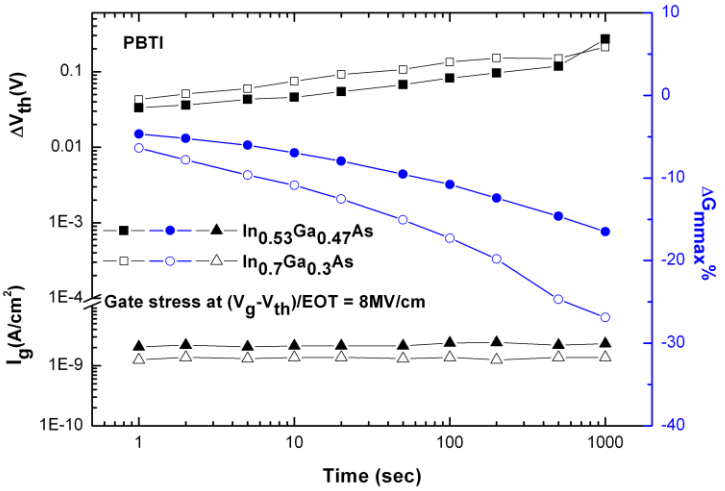


Figure 2.13. V_{th}, G_{mmax} and I_g change during PBTI stress at effect electrical field 8MV/cm of $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ MOSFETs with Al_2O_3 oxide.

PBTI measurement results were shown in Figure 2.13. V_{th}, G_{mmax} and I_g change was measured at stress of 8MV/cm. Similar slope of V_{th} versus time of $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ MOSFETs indicates that both oxide and III-V interfaces have similar trap

trapping behavior. $In_{0.7}Ga_{0.3}As$ MOSFETs exhibit larger amount of interface degradation shown from G_{mmax} change. The gate leakage current is similar for both devices.

In summary, InGaAs surface channel MOSFETs with ALD gate dielectrics were fabricated and investigated here. Peak mobility of $1600cm^2/Vs$ was achieved using $In_{0.53}Ga_{0.47}As$ channel MOSFETs with Al_2O_3. $In_{0.53}Ga_{0.47}As$ MOSFETs were found to exhibit better device performance than $In_{0.7}Ga_{0.3}As$ MOSFETs including higher transconductance, higher mobility and lower subthreshold swing for both Al_2O_3 and ZrO_2 gate dielectric (e.g. SS for $In_{0.53}Ga_{0.47}As$ is 125 mV/dec for Al_2O_3 vs. 160 mV/dec for $In_{0.7}Ga_{0.3}As$). D_{it} measured by conductance method indicates lower interface trap density at $In_{0.53}Ga_{0.47}As$/oxide interface (1.1×10^{12} $eV^{-1}cm^{-2}$ for $In_{0.53}Ga_{0.47}As$ vs. 3.2×10^{12} $eV^{-1}cm^{-2}$ for Al_2O_3). Capacitance-Voltage measurement at 77 K also correlates with the above results showing smaller frequency dispersion for $In_{0.53}Ga_{0.47}As$ devices.

Chapter 3: Buried Channel InGaAs MOSFETs

Although high effective channel mobility of 1600cm^2/Vs was achieved by surface channel InGaAs MOSFETs, it is still far away from reaching its potential intrinsic mobility. The degradation is mainly due to scattering of interface traps at high-k oxide and III-V channel interface. Buried channel MOSFETs were designed to enhance the effective channel mobility by adding a thin barrier layer on top of channel. In this way, the problematic oxide/III-V interface is kept away from effective channel region. The degradation of interface trap scattering is largely reduced. Compared to surface channel device, buried channel structure improves mobility significantly [71][72]; Compared to HEMT structure, buried channel device exhibit the advantage of reduced gate leakage current by providing a high-k dielectric to the gate stack [73][74]. However, the tradeoff is that by adding the barrier layer, the gate to channel distance is increased, leading to a reduced gate control over the channel. This may potentially degrade the short channel device performance. In this chapter, device performances of buried channel InGaAs MOSFETs were investigated while surface channel InGaAs MOSFETs were used as control samples. InGaAs buried channel devices with various barrier layer materials and thicknesses have been fabricated and compared in term of drive current, transconductance and effective channel mobility. Improved on-state performance was achieved compare to surface channel devices by utilizing InP and InAlAs as barrier layer. Devices with 1nm InP barrier exhibit around 60% increase in drive currant and effective channel mobility. With thicker barrier layer, drive current and mobility were further enhanced. Devices with InP/InAlAs double barrier show highest drive current and effective channel mobility.

3.1. BURIED CHANNEL INGAAS MOSFETS WITH VARIOUS BARRIER LAYERS

The schematic cross section of an InGaAs buried channel MOSFET is shown in Figure 3.1. The layer structure was grown by MBE on 3-inch semi-insulating InP substrate, followed by 300nm $In_{0.52}Al_{0.48}As$ buffer layer, 10nm quantum well $In_{0.7}Ga_{0.3}As$ channel, a thin barrier layer (sample#1: 1nm InP, sample#2: 3nm InP, and sample#3:1.5nm $In_{0.52}Al_{0.48}As$/2nm InP double barrier) and a 20nm N+ InGaAs cap layer. All the layers were designed to be undoped except for the top N+ $In_{0.53}Ga_{0.47}As$ layer. Several aspects need to be considered when select the barrier material and thickness: 1) the lattice mismatch between layers and MBE feasibility; 2) wet etch selectivity in fabrication process; 3) band alignment of barrier and channel; 4) interface quality of high-k and barrier layer; 5) interface quality of barrier and channel layer. InP was chosen as the top barrier layer because InP is lattice matched to the substrate. It also performed as an etch-stop layer and was used to improve the oxide interface quality (i.e. Dit of oxide/InP interface is lower than that of oxide/InAlAs interface). However, the conduction band offset of InP/InGaAs (~0.25eV) is not large enough to prevent electrons from spilling over at high gate electric field. InAlAs was added because of its wide bandgap. The conduction band offset for InAlAs/InGaAs is around 0.5eV, which can better confine carriers in the channel.

Buried channel MOSFETs were fabricated by first forming gate recess using citric acid based wet etch. For devices without barrier layer, InP layer was removed by diluted hydrochloric acid wet etch. Gate dielectric was grown directly on III-V surface by ALD after cleaning and surface passivation. TaN was deposited as gate electrode by sputtering. Source and drain ohmic contact was formed by e-beam evaporation of PdGe and rapid thermal anneal at 320℃ for 30s. Long-channel ring-typed devices (Lg=20μm) were fabricated to enable mobility calculation.

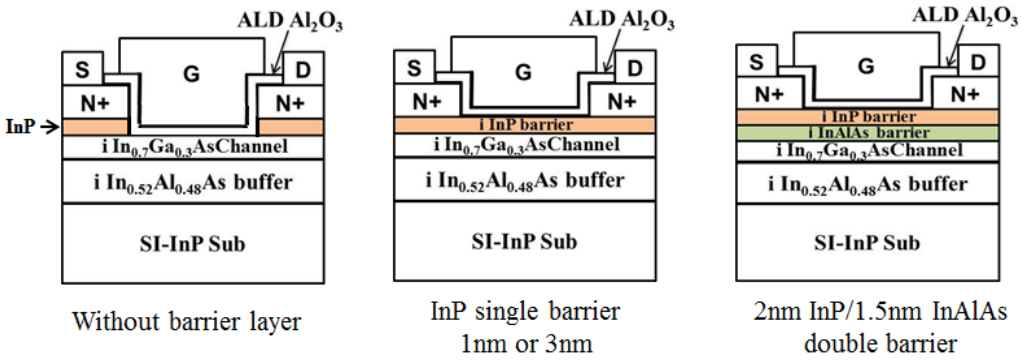


Figure 3.1. Schematic view of $In_{0.7}Ga_{0.3}As$ buried channel MOSFET with InP or InP/InAlAs barrier layer.

The drive current and extrinsic transconductance of devices without barrier layer, with 1nm InP, 3nm InP and InP/InAlAs double barrier are compared in Figure 3.2. Devices with barrier layer show higher drive current and transconductance than devices without barrier layer. For devices with 3nm InP barrier layer, the drive current goes down slightly at high gate voltage. This is due to electron spill over into the lower mobility barrier layer at high electrical field. Devices with InP/InAlAs double barrier exhibit the highest drive current and transconductance. Since the conduction band offset of $In_{0.52}Al_{0.48}As/In_{0.7}Ga_{0.3}As$ is higher than $InP/In_{0.7}Ga_{0.3}As$, electrons can be better confined in InGaAs channel layer with the added InAlAs barrier layer. Figure 3.3 illustrates the extrinsic transconductance characteristics as a result of vertical scaling of gate dielectric.

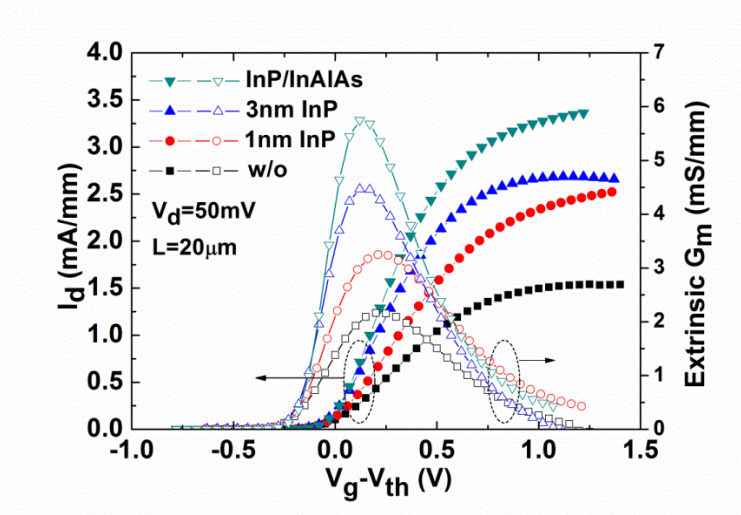


Figure 3.2. I_d-V_g and extrinsic G_m-V_g at V_d =50mV for $In_{0.7}Ga_{0.3}As$ MOSFETs with different barrier materials.

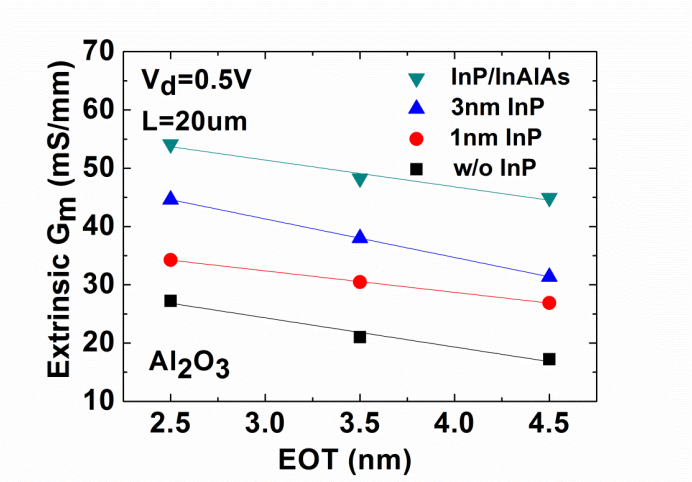


Figure 3.3. Extrinsic G_m for $In_{0.7}Ga_{0.3}As$ MOSFETs with different barrier materials as a function of EOT at V_d=0.5V.

The gate leakage current for all the devices is less than 6×10^{-9}A/cm^2 at Vg=1V for Al_2O_3 at EOT of 4.4nm. The off-state current is similar for these devices, with I_{off} of around 5×10^{-6} mA/mm at V_g=-1V and V_{ds}=50mV (Figure 3.4). Subthreshold swing

characteristic of InGaAs MOSFETs with vertical scaling of the gate dielectric Al_2O_3 is shown in Figure 3.4 inset. For Al_2O_3 at EOT=4.4nm, the subthreshold swing of devices with 1nm InP or 3nm InP are around 110mV/dec. The InP/InAlAs double barrier devices show slightly smaller swing of 104mV/dec. This is believed to be due to the MBE growth dynamic which leads to a better interface quality of InAlAs/InGaAs than InP/InGaAs. Also, the 1nm thick InP layer may not be thick enough to act as wet etch stop layer. Devices without barrier layer show the smallest subthreshold swing of about 98mV/dec.

The output characteristics of buried channel InGaAs MOSFETs are compared to devices without barrier layer (see Figure 3.5). Drive current was measured at V_g-V_{th}=0 to 2V with a step of 0.5V. With 1nm InP, the drive current (for L_g=20μm) show an increase from 52mA/mm to 83mA/mm at V_g-V_{th}=2V. The maximum drive current at V_g-V_{th}=2V for double barrier InGaAs MOSFETs is ~123mA/mm. The maximum drive current was enhanced with increased barrier layer thickness. This is due to a larger distance between InGaAs channel and the gate dielectric interface and thus the channel carriers are less affected by the interface trap scattering. With higher mobility, devices with thicker barrier layer show higher drive current. Source resistance of devices without barrier layer is larger than that of devices with barrier layer. This is because devices without barrier still possess InP layer at source and drain region. The wet etching process may under-cut at InP layer. Due to the current crowding effect near the gate region, the source and drain resistance is dominated by the corner effect. One trade-off of adding a barrier layer is that source and drain resistance will be increased. This will degrade the on-state performance, especially for sub-micron gate length devices.

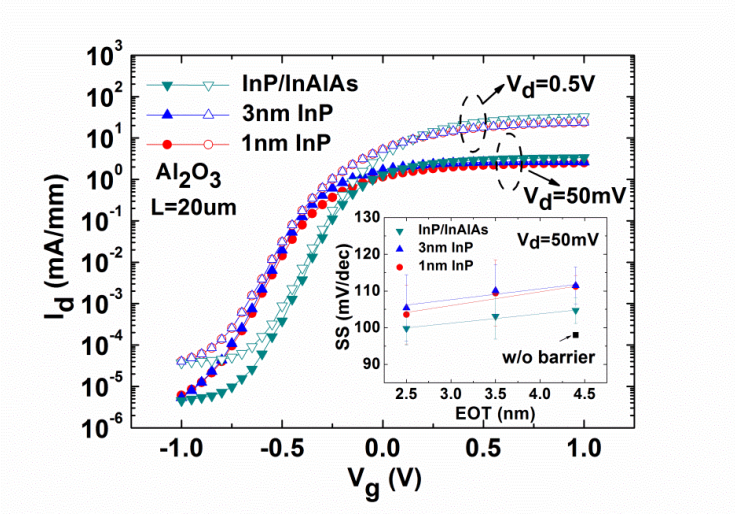


Figure 3.4. Log(I_d)-V_g for $In_{0.7}Ga_{0.3}As$ buried channel MOSFETs with 1nm InP, 3nm InP and InP/InAlAs double barrier layer. Subthreshold swing characteristic of vertical scaling of gate dielectric was inserted.

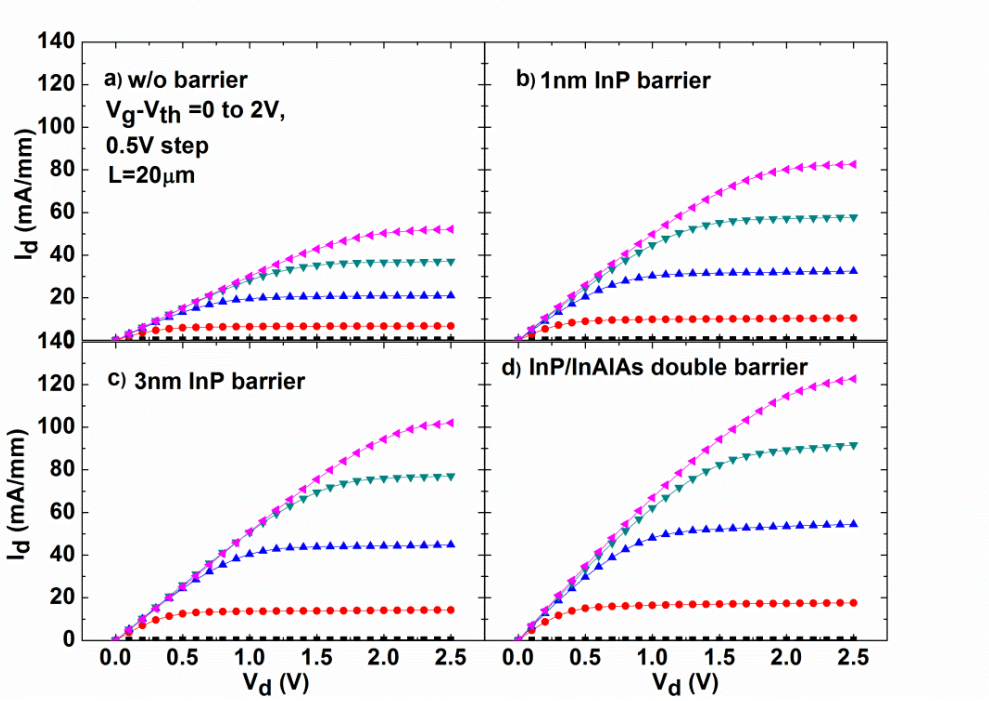


Figure 3.5. Output characteristics of $In_{0.7}Ga_{0.3}As$ channel MOSFETs with Al_2O_3 gate dielectric.

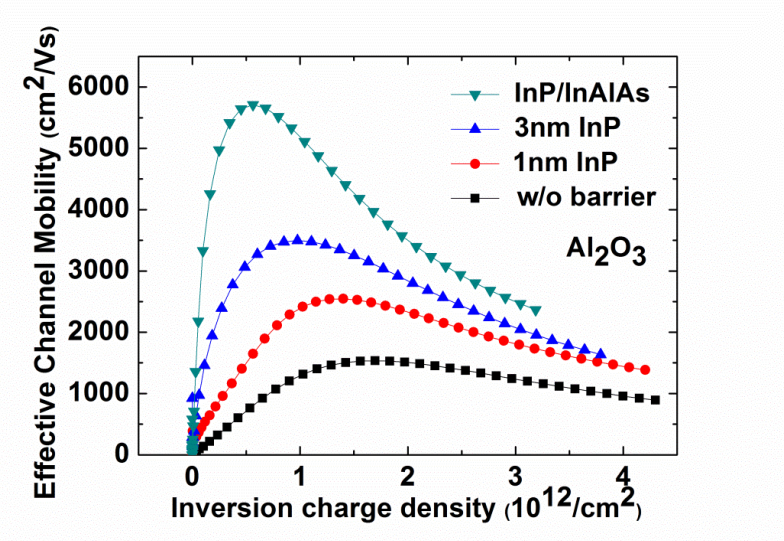


Figure 3.6. Effective channel mobility measured using split CV method for $In_{0.7}Ga_{0.3}As$ channel MOSFETs

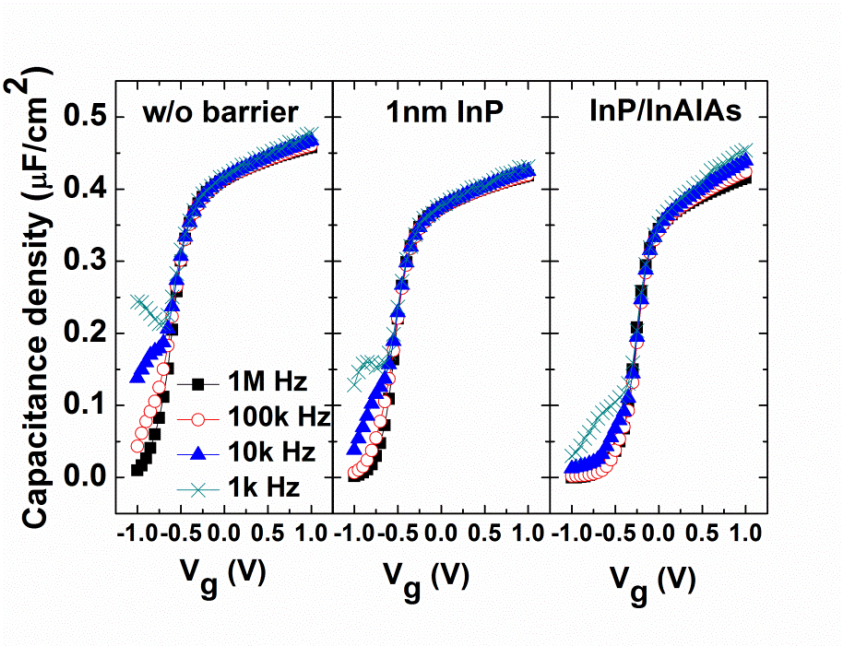


Figure 3.7. CV measurements of InGaAs channel MOSFETs

Effective channel mobility of InGaAs MOSFETs with different barrier layers was measured using split CV method (see Figure 3.6). The extracted channel mobility is consistent with I_d and G_m performance. The highest effective channel mobility around 5700cm^2/Vs was achieved by InP/InAlAs double barrier devices at inversion charge density of $0.5\times10^{12}/cm^2$. Compared to devices without barrier, by adding 1nm InP barrier layer, the peak mobility and high electrical field mobility (at inversion charge density of $4\times10^{12}/cm^2$) is increased by 65% and 51% respectively. The results show that the effective channel mobility is sensitive to the interface/carrier distance. Figure 3.7 illustrates the multi-CV characteristics measured from long channel devices (L_g=20μm) at 1 MHz, 100 kHz, 10 kHz and 1 kHz. Interface trap density (D_{it}) was extracted using conductance method. D_{it} of Al_2O_3/InP and Al_2O_3/InGaAs are comparable and of around 1×10^{12} $ev^{-1}cm^{-2}$. CV and D_{it} characteristics indicate that oxide interface quality of these devices is similar.

The above results show that by applying 1nm InP barrier layer, the drive current, extrinsic transconductance and effective channel mobility were all improved, compared to devices without barrier layer. For thicker barrier, the drive current, transconductance and mobility were further improved by keeping channel further away from oxide/III-V interface. For devices with 3.5nm InP/InAlAs double barrier, CET is increased by ~1nm while the drive current and effective channel mobility are significantly improved.

2.2. SCALING BEHAVIOR OF INGAAS MOSFETS

While the buried channel MOSFETs structure improved the on-state performance significantly, the tradeoff is that by adding the barrier layer, the gate to channel distance is increased, leading to a reduced gate control over channel. This may potentially degrade the short channel device performance. In this section, the scaling behavior of buried channel InGaAs MOSFETs down to sub-50nm regime has been discussed and compared to surface channel InGaAs MOSFETs.

The cross-sectional schematic view of short channel $In_{0.7}Ga_{0.3}As$ buried-channel MOSFETs is shown in Figure 3.8 (a). Figure 3.8 (b) and (c) show the SEM image of top view (for L_g=40nm device) and cross-sectional view (for L_g=100nm device) of the $In_{0.7}Ga_{0.3}As$ MOSFET gate region, respectively. The layer structure was the same as in Figure 3.1. The key fabrication steps of short-channel buried-channel MOSFETs were the same as long channel devices. The entire lithography steps were done by e-beam lithography. After mesa etching, the gate was patterned by diluted photoresist ZEP520 to enable small size of 40nm. The gate recess was then done using citric acid based wet etch, which was optimized in order to minimize non-uniformity and line edge roughness. For devices without barrier, the 1nm InP barrier layer was removed by a quick dip in diluted HCl. A 6nm Al_2O_3 (i.e. EOT of 2.5nm) was deposited as gate dielectrics after surface cleaning and passivation. TaN was sputtered as gate metal. Metal gate area was then defined by e-beam lithography and CF_4 RIE using Al_2O_3 as the hard mask. Sources and drain metal was deposited using lift-off process with Pd/Ge/Ti/Pd stack. Source/Drain to gate distance is 1um. All the alignment for e-beam process was done by applying Pd (around 1500nm) as marks at the first step. MOSFETs with active gate length from 40nm to 1um were fabricated. Note that these are actual gate length values measured by SEM.

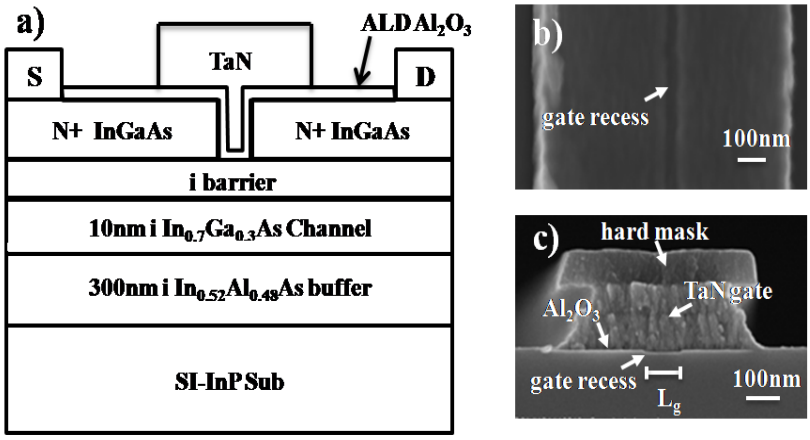


Figure 3.8. (a) Cross-sectional schematic view of $Al_2O_3/In_{0.7}Ga_{0.3}As$ MOSFET with barrier layer of InP or InAlAs. (b) SEM image showing the top view of 40nm gate length $In_{0.7}Ga_{0.3}As$ MOSFET. (c) SEM image of the cross-sectional view of the 100nm gate length $In_{0.7}Ga_{0.3}As$ MOSFET.

The drive current and extrinsic transconductance of short-channel $In_{0.7}Ga_{0.3}As$ MOSFETs (L_g=40nm) without barrier layer, with InP barrier and InP/InAlAs double barrier were compared in Figure 3.9. Devices with barrier layer show more than 2X higher drive current than devices without barrier layer resulting from improved channel mobility (see Figure 3.6). The devices with InP/InAlAs double barrier show the highest mobility (~2500cm^2/Vs at inversion charge density of $3\times10^{12}/cm^2$) in comparison to the devices with 1nm InP barrier (~1800cm^2/Vs) and those without barrier layer (~1230cm^2/Vs). $In_{0.7}Ga_{0.3}As$ MOSFETs with InP/InAlAs double barrier exhibit the highest drive current and extrinsic transconductance.

Figure 3.10 illustrates the subthreshold characteristics of short-channel InGaAs MOSFETs. For 40nm gate length, devices without barrier layer exhibit smaller SS (103mV/dec) than devices with 1nm InP and devices with InP/InAlAs double barrier due to lower CET. The subthreshold swing is slightly better for devices with double barrier

(130mV/dec) than devices with single InP barrier (140mV/dec). The higher off-state current for devices with thicker barrier might be due to the reduced gate control over channel. The interface quality of the long-channel devices is believed to be the same as that of the short-channel devices because both undergo the exact same process flow.

The output characteristics of the 40nm gate length $In_{0.7}Ga_{0.3}As$ MOSFETs are illustrated in Figure 3.11. MOSFETs with 1nm InP barrier exhibits the highest drive current of 690mA/mm at V_g-V_{th}=1.4V. The maximum drive current of devices with double barrier is lower than devices with InP single barrier. This is believed to be due to the larger S/D resistance for the double-barrier MOSFETs. The thicker barrier layer and the increased barrier heights contribute to the increase in S/D resistance.

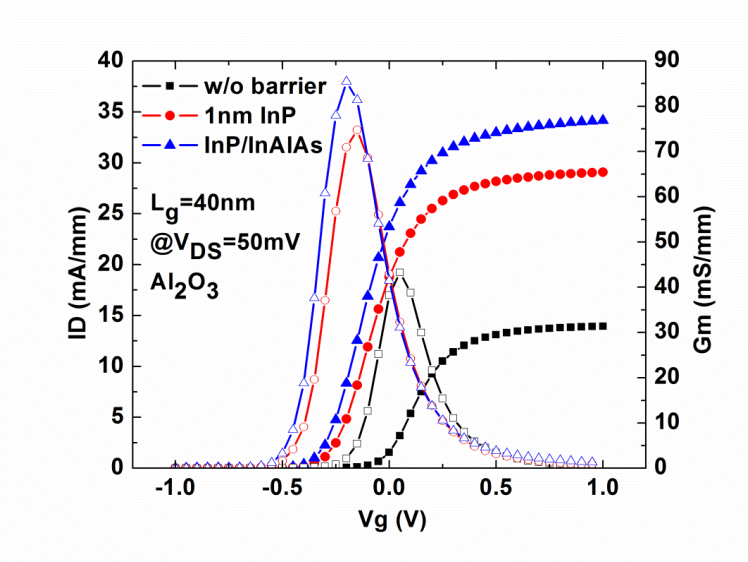


Figure 3.9. Transfer characteristics of $In_{0.7}Ga_{0.3}As$ MOSFETs without barrier layer, with 1nm InP barrier layer and with InP/InAlAs barrier layer.

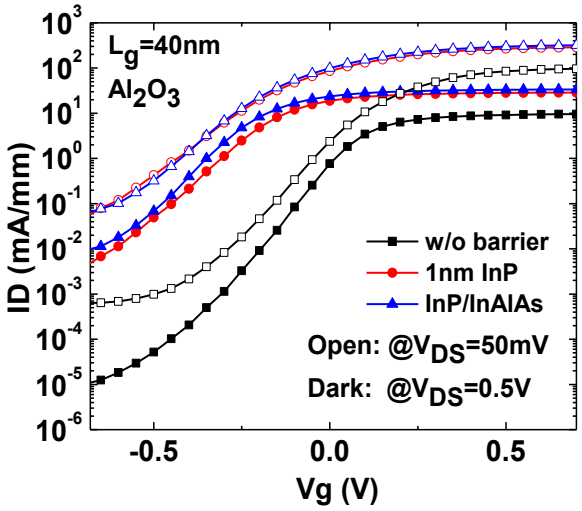


Figure 3.10. Subthreshold characteristics of $In_{0.7}Ga_{0.3}As$ MOSFETs without barrier layer, with 1nm InP barrier layer and with InP/InAlAs barrier layer.

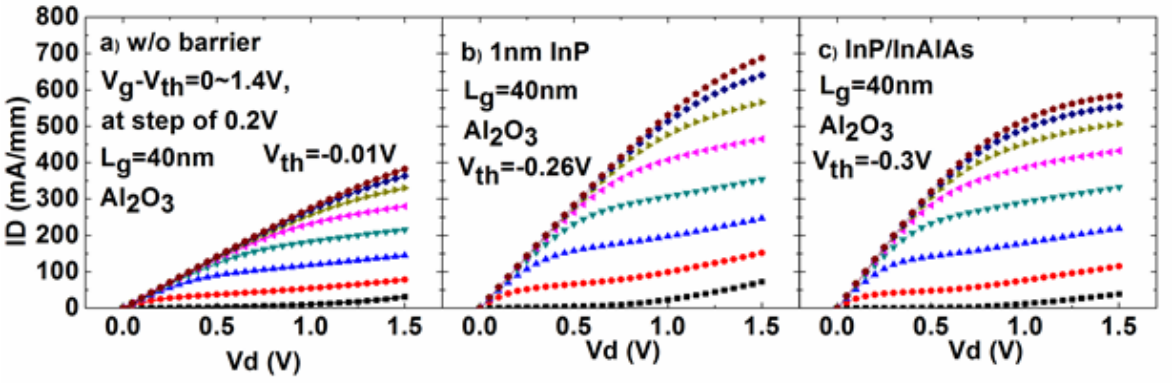


Figure 3.11. I_{DS}-V_{DS} output characteristics of 40nm gate length $In_{0.7}Ga_{0.3}As$ MOSFET (a) without barrier layer, (b) with 1nm InP barrier layer, (c) with InP/InAlAs barrier layer.

Figure 3.12 shows the extrinsic transconductance of $In_{0.7}Ga_{0.3}As$ MOSFETs with and without barrier layer as a function of gate length. At V_{ds}=1V, devices with barrier layer exhibit almost two times higher extrinsic transconductance than devices without

barrier layer. MOSFETs with InP/InAlAs double barrier exhibit transconductance of 570mS/mm at V_{ds}=1V for L_g=40nm. Transconductance are comparable for 1nm InP barrier and InP/InAlAs double barrier. At V_{ds}=0.5V, devices with double barrier show slightly higher transconductance than devices with 1nm InP barrier layer. The source resistances extracted from the gate length dependence show around 1500 ohm-μm for devices with barrier layer (InP single and double barrier), and around 3000 ohm-μm for devices without barrier layer. The higher source resistance of devices without barrier is due to the undercut of InP layer at source and drain region. For 40nm devices, it is difficult to accurately extract the channel resistance because it is much smaller than the source resistance. The higher on-resistance of surface channel devices results from its lower channel mobility and higher source resistance. Improving the S/D contact process and reduced S/D resistance can further improve the drive current and extrinsic transconductance.

The SS and DIBL vs. gate length were plotted in Figure 3.13 and Figure 3.14, respectively. The DIBL for the device (L_g=40nm) with double barrier and without barrier layer are 175mV/V and 131mV/V. The smaller DIBL is believed to be due to the smaller gate-to-channel distance. Devices with double barrier exhibit lower DIBL than devices with single InP barrier. This might result from a better interface at InAlAs/InGaAs than InP/InGaAs. Better gate control can be achieved by shrinking oxide thickness or using higher k value dielectric material to compensate for the short channel effect.

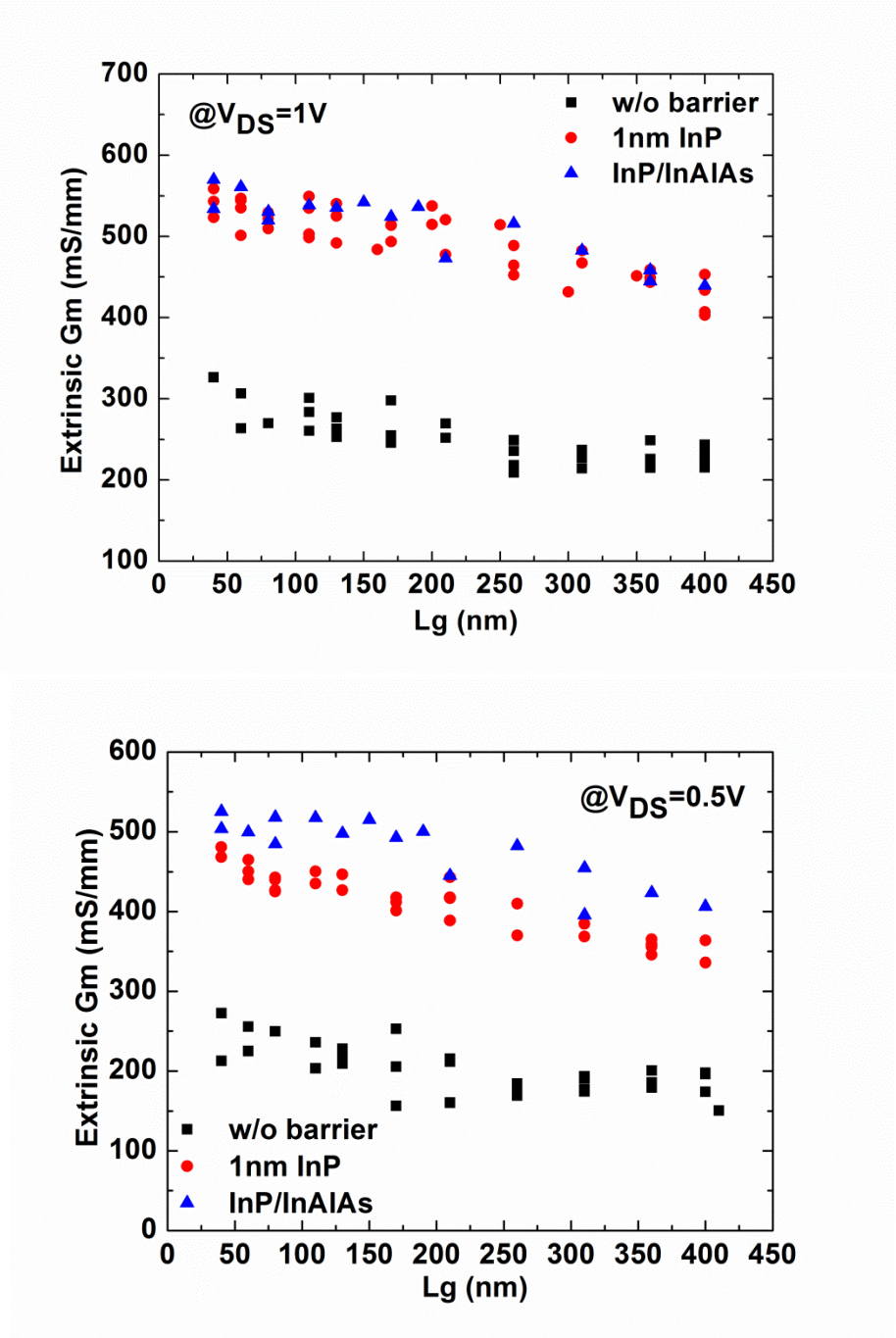


Figure 3.12. Extrinsic transconductance of $In_{0.7}Ga_{0.3}As$ MOSFETs as a function of gate length at V_{ds}=1V and 0.5V.

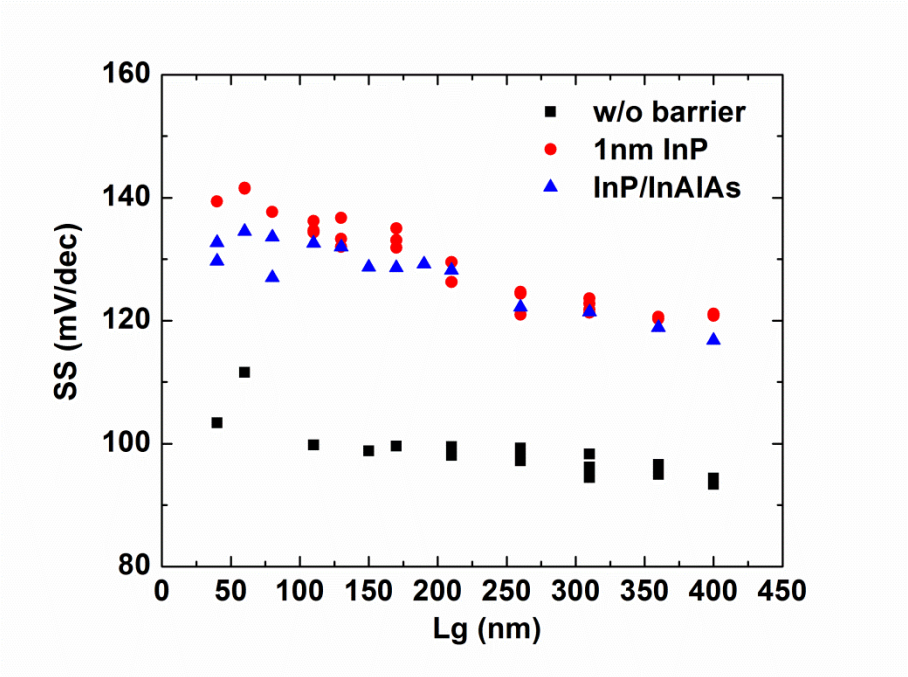


Figure 3.13. SS versus gate length of $In_{0.7}Ga_{0.3}As$ MOSFETs

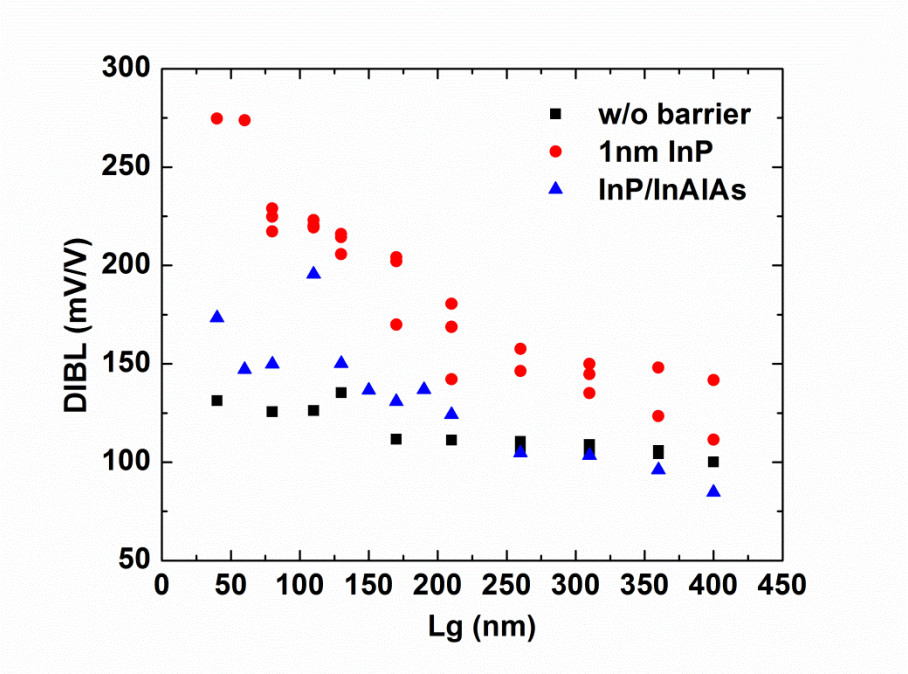


Figure 3.14. DIBL versus gate length of $In_{0.7}Ga_{0.3}As$ MOSFETs

Tabel 3.1. Summary of InGaAs MOSFETs

Device structure*	I_{ON} (mA/mm) @V_{GS}=1V, V_{DS}=1V	G_m (mS/mm) @V_{DS}=1V	μ_{eff} (cm^2/vs) @$3\times10^{12}/cm^2$	SS (mV/dec) @V_{DS}=0.05V	DIBL (mV/V) @I_D=1mA
w/o	185	326	1230	103	131
1nm InP	500	558	1800	140	274
InP/InAlAs	498	570	2500	130	173

*L_g=40nm, W=100μm

Table 3.1 summarized the device performance of InGaAs channel MOSFETs. Good scaling behavior has been observed for III-V MOSFETs. $In_{0.7}Ga_{0.3}As$ channel devices with barrier layer exhibit much higher drive current and transconductance (for L_g=40nm InP/InAlAs double barrier device, G_m=570mS/mm at V_{ds}=1V) than devices without barrier layer (for L_g=40nm, G_m=330mS/mm at V_{ds}=1V). Subthreshold swing and DIBL are lower for devices without barrier layer (for L_g=40nm device, SS=103mV/dec, DIBL=131mV/V). The buried channel devices have better on-state but worse off-state properties than surface channel devices. By utilizing III-V high-k, the gate stack can be tailored to achieve the optimum performance for different application.

2.3. Dependence of Channel Thickness

As the transistor scaled down laterally to reduce the area as well as improve device performance, the vertical dimension needs to be scaled at the same time. One way to scale the device vertically is by shrinking the EOT of gate dielectric. With a smaller EOT, gate have better control over channel thus short channel effect is reduced. The concomitant of shrinking EOT is the increase of gate leakage current. Another way is to reduce the channel thickness. In this section, impact of channel thickness dependence of

nano-scaled $In_{0.7}Ga_{0.3}As$ QWFETs with high-κ gate dielectrics was investigated. $In_{0.7}Ga_{0.3}As$ QWFETs with 5 nm and 10 nm thick channel layer have been fabricated and analyzed. The 5 nm $In_{0.7}Ga_{0.3}As$ channel (L_g= 40 nm) devices exhibit a reduced SS of around 100 mV/dec and DIBL of 128 mV/V compared to 10 nm $In_{0.7}Ga_{0.3}As$ channel devices (SS ~140 mV/dec, DIBL ~275 mV/V). However, the drawback for thinner channel devices is that the effective channel mobility also decreases. At inversion charge density of $3\times10^{12}/cm^2$, 10 nm $In_{0.7}Ga_{0.3}As$ channel devices exhibit mobility of 1860 cm^2/Vs vs. mobility of 1460 cm^2/Vs for 5 nm $In_{0.7}Ga_{0.3}As$ channel devices. Device performances figures of merit including drive current, transconductance, subthreshold swing and effective channel mobility have been compared.

The layer structure is the same as in the previous section with 1nm InP barrier layer. Two channel thicknesses were examined (i.e. 5nm and 10nm for sample #1 and #2, respectively). 6 nm Al_2O_3 (i.e. equivalent oxide thickness, EOT of 2.5 nm) was deposited as gate dielectric. Figure 3.15 illustrates the I_d-V_g characteristics of the InGaAs MOSFETs at Vds=0.05V and 0.5V. The on/off current ratios for 5 nm and 10 nm thick channel InGaAs MOSFETs are around 3×10^3 and 4×10^2 respectively. On/off current ratio is defined here as I_{on} at $V_g=V_{th}+2/3V_d$ and I_{off} at $V_g=V_{th}-1/3V_d$, V_d=0.5V [75]. As the channel layer thickness decreases from 10 nm to 5 nm, the threshold voltage V_{th} increases (i.e. from -0.26 V to -0.1 V). V_{th} increase for thinner channel may due to a stronger quantum confinement in thinner channel where the ground state energy level is higher. V_{th} roll-offs for the 5nm and 10nm thick-channel devices are 30mV and 80mV, respectively. The gate leakage current for both devices is around 1×10^{-5} mA/mm. The linear plot of drive current and transconductance characteristics of InGaAs MOSFETs at V_{ds}=0.5V are illustrated in Figure 3.16.

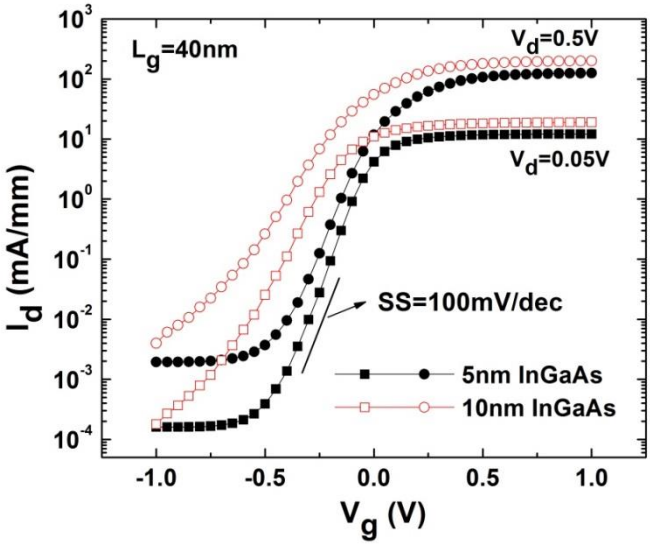


Figure 3.15. Subthreshold and gate current characteristics of $In_{0.7}Ga_{0.3}As$ QWFETs with 5nm and 10nm channel measured at V_{ds}=0.05V and 0.5 V.

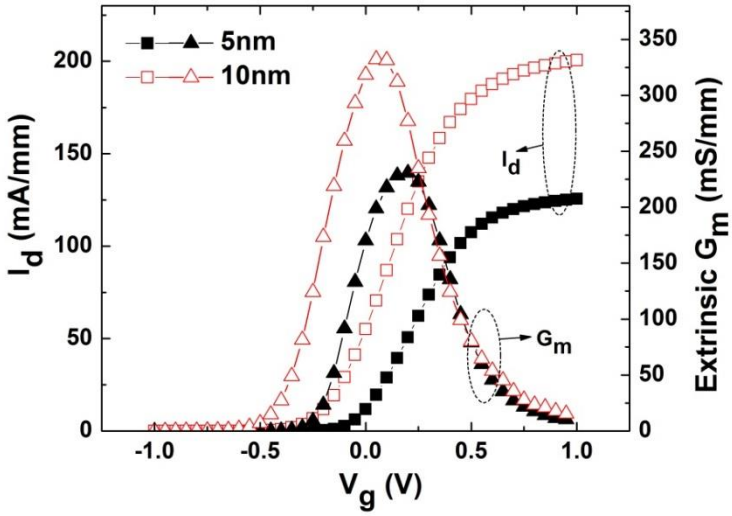


Figure 3.16. I_d and transconductance characteristics of $In_{0.7}Ga_{0.3}As$ QWFETs with 5nm and 10nm channel measured at V_{ds}= 0.5 V.

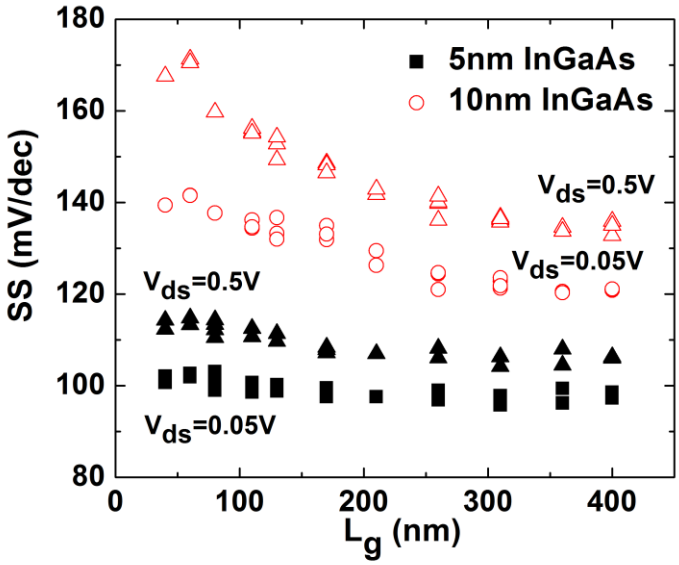


Figure 3.17. Subthreshold vs. gate length characteristics of $In_{0.7}Ga_{0.3}As$ QWFETs at V_{ds}=0.05V and 0.5V

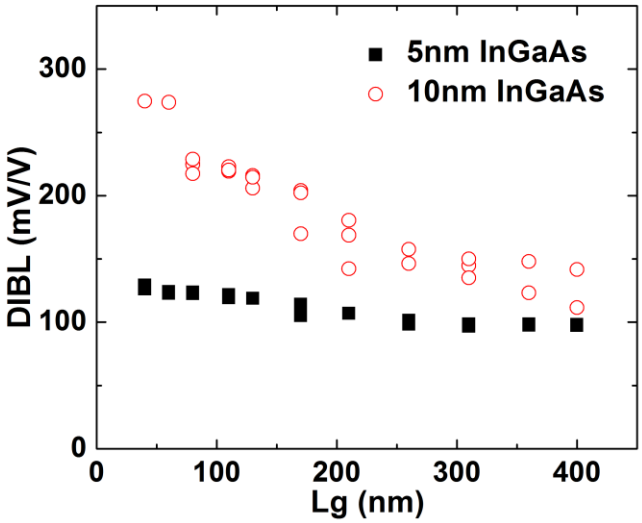


Figure 3.18. DIBL vs. gate length of $In_{0.7}Ga_{0.3}As$ QWFETs

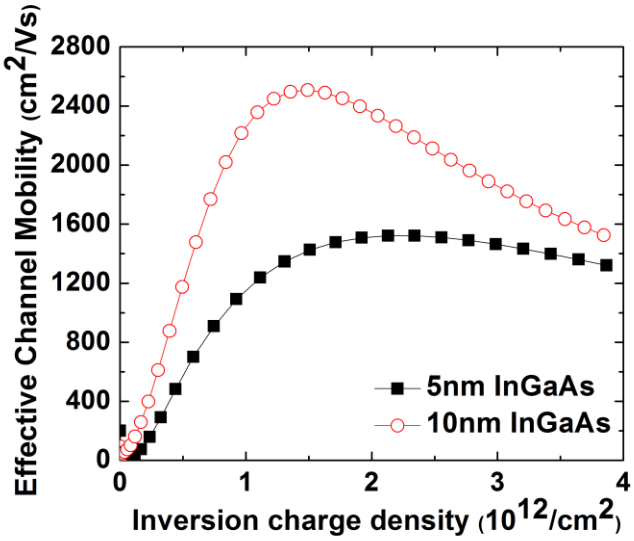


Figure 3.19. Effective channel mobility measured using split-CV method for 5nm and 10nm channel $In_{0.7}Ga_{0.3}As$ QWFETs.

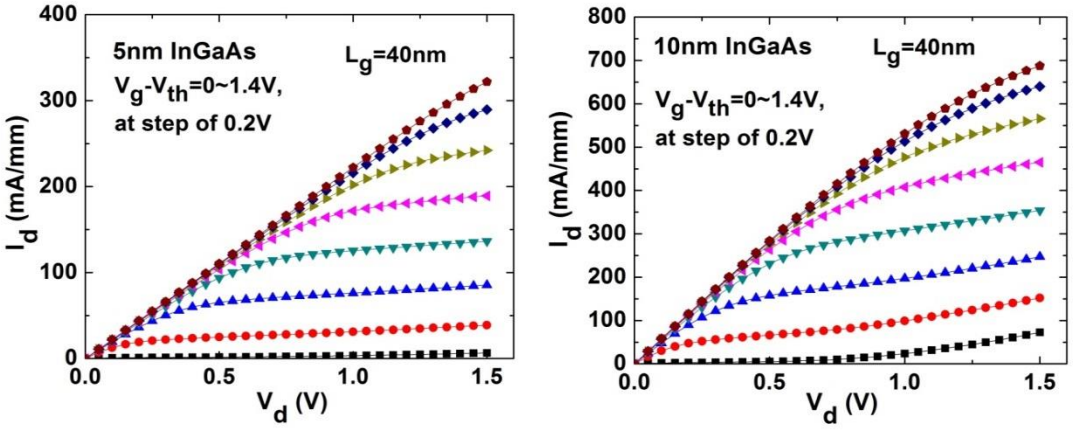


Figure 3.20. I_d-V_d output characteristics of $In_{0.7}Ga_{0.3}As$ QWFET with 5nm and 10nm thick channel.

Improved subthreshold swing can be observed for thinner channel devices (Figure 3.15). As the device channel thickness is reduced from 10 nm to 5 nm, subthreshold swing improves from 140 mV/dec to 100 mV/dec. One possible explanation is that for depletion mode MOSFETs, the effective distance between the conductive channel and the gate electrode decreases for thinner channel device due to a reduced depletion region. Subthreshold swing vs. gate length is plotted in Fig. 3.17. The subthreshold swing of the 5nm InGaAs MOSFET remain relatively unchanged as the gate length reduces from 400 nm (SS~98mV/dec) to 40 nm (SS~100mV/dec), while the subthreshold characteristics for the 10nm channel devices start to degrade when gate length drops below 200 nm. Reduced subthreshold swing roll-up for thinner channel devices is due to improved SCE control. Interface trap density of around 1.5×10^{12}/eV/cm^2 was extracted using conductance method for Al_2O_3/InP interface at room temperature.

Figure 3.18 illustrates DIBL vs. gate length as a function of channel thickness. DIBL is measured at I_{ds} = 1 mA/mm and V_{ds} at 0.05V and 0.5V. The results show that thinner channel devices exhibit improved DIBL characteristics and reduced SCE. This is because for thinner channel devices, the depletion region thickness is reduced; and the gate electrode is better coupled to the conductive channel.

Effective channel mobility (Figure 3.19) is extracted using split-CV measurement on long-channel devices. The measured peak mobility are ~1520 cm^2/Vs and ~2500 cm^2/Vs for 5nm and 10 nm thick channel $In_{0.7}Ga_{0.3}As$ MOSFETs, respectively. The mobility of 5nm and 10nm thick channel devces become similar at high inversion charge density. One possible mechanism for the reduced mobility for thinner channel is an increased phonon scattering due to stronger carrier confinement. Further studies on mobility degradation is needed. At low carrier concentration, carrier distribution is closer to the gate oxide for thinner channel devices leading to increased interface scattering. At

higher carrier concentration, carrier distribution for 5 nm channel and 10 nm channel devices converges.

The current drive capability of 5nm and 10nm channel MOSFETs is shown in Figure 3.20. The extrernal resistance was extracted using gate length dependence measurement. The source resistance for devices with 10nm and 5nm channel are around 1.1 ohm-mm and 1.5 ohm-mm, respectively. High source resistance may be due to the InP barrier layer at source and drain region and the large source/drain to gate distance. Contact fabrication process needs to be further optimized in order to improve the current drive characteristics of our devices.

From the above analysis, thinner channel (5 nm) $In_{0.7}Ga_{0.3}As$ devices exhibit better subthreshold swing and improved short channel effect control. The drawbacks for thin channel devices are reduced effective channel mobility and current drive. The thinner channel QWFETs exhibit potential to scaling to smaller dimension.

2.4. INAS INSERTED INGAAS CHANNEL

InAs has been considered a potential channel material to provide better performance with an electron mobility as high as 20,000cm^2/Vs at room temperature. However, the main challenge is, as in most cases of III-V devices, finding a high-quality dielectric and semiconductor interface. It has been reported that the interface states invert the p-InAs surface to n type [76] and InAs/oxide device can hardly be cut off because of the band-to-band tunneling current [77]. Buried channel MOSFETs is one solution to this problem where a barrier layer is added on the top of channel layer. InAs HEMTs have recently been reported to achieve excellent device performance [74]. However, for III-V

based field effect transistors applicable in ULSI CMOS circuits, high-k dielectrics are needed in the gate stack to overcome the gate leakage problem. Thus here InAs buried channel MOSFETs with ALD gate dielectrics were fabricated and investigated. Two different InAs MOSFET structures were studied with InAs inserted on the top of the channel (InAs/InGaAs channel) and InAs inserted in the middle of the channel (InGaAs/InAs/InGaAs channel). The device structure of InAs inserted on the top of the channel is designed to reduced gate to channel distance and thus improve gate control over channel. The comparison of InAs MOSFETs and pure $In_{0.7}Ga_{0.3}As$ channel buried channel devices was also studied. Both InAs MOSFETs show good off-state and saturation properties. Devices with InAs on top exhibit lower drive current and effective channel mobility than pure InGaAs channel devices. However, by moving InAs layer into the middle of InGaAs channel and increasing the barrier layer thickness, the effective channel mobility was increased by two times. The channel mobility is not only sensitive to high-k/III-V interface but also InAs/InAlAs interface.

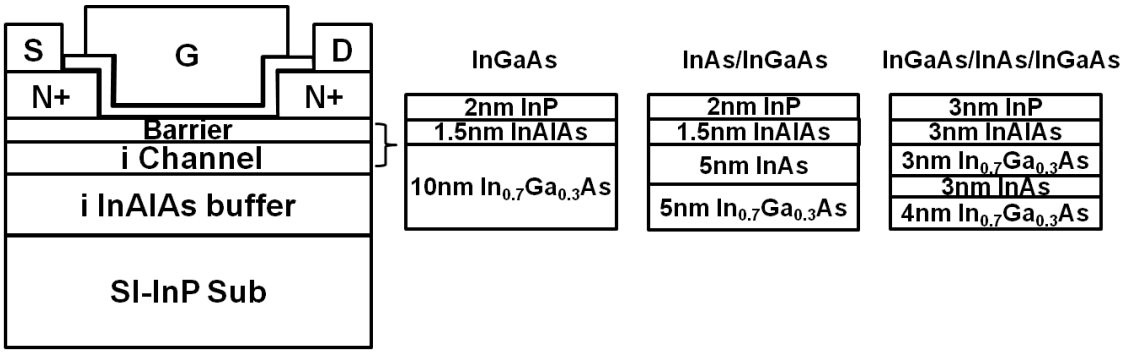


Figure 3.21. Cross-sectional schematic view of InGaAs and InAs inserted buried channel MOSFETs with ALD gate dielectric.

The layer structure of InAs and InGaAs MOSFETs are shown in Figure 3.21. All the samples were grown by MBE on 3-inch semi-insulating InP substrate followed by 300nm $In_{0.52}Al_{0.48}As$ buffer layer, 10nm quantum well channel (pure $In_{0.7}Ga_{0.3}As$ channel for sample #1, 5nm $In_{0.7}Ga_{0.3}As$/5nm InAs channel for sample #2, 4nm $In_{0.7}Ga_{0.3}As$/3nm InAs/3nm $In_{0.7}Ga_{0.3}As$ for sample #3), InAlAs/InP double barrier and a 20nm n+ InGaAs cap layer. Fabrication process can be found in previous section 3.1.

The drive current and extrinsic transconductance of InAs/InGaAs channel, InGaAs/InAs/InGaAs channel and pure InGaAs channel MOSFETs were compared in Figure 3.22. The gate leakage current for all the devices is less than $8\times10^{-5}A/cm^2$ at V_g=1V. InAs in the middle InGaAs/InAs/InGaAs buried channel devices exhibit the highest drive current and extrinsic transconductance. Compare to pure InGaAs channel, InGaAs/InAs/InGaAs channel devices show 21% increase in drive current and 8% increase in maximum transconductance. By moving InAs layer to the top of the channel, as the interface with the top barrier is different, InAs InAs/InGaAs channel MOSFETs actually show smaller drive current and transconductance. This is possibly due to crystalline defect at InAlAs/InAs interface.

Figure 3.23 shows the $\log(I_d)$-V_g characteristics of InAs and InGaAs buried channel devices with 8nm Al_2O_3 (effective oxide thickness (EOT) around 4.4nm). Devices with InAs inserted in the middle (i.e. InGaAs/InAs/InGaAs structure) exhibit good off-state property with on-off current ratio around 1.2×10^4, which is similar as the pure InGaAs channel MOSFETs. InAs on the top InAs/InGaAs channel devices show one order lower on-off current ratio but the MOSFETs can still be well cut off. The

subthreshold swing of pure InGaAs channel devices is 99mV/dec at V_{ds}=50mV. The InGaAs/InAs/InGaAs channel devices show slightly higher subthreshold swing of 107mV/dec. Although the InGaAs/InAs/InGaAs channel devices has thicker barrier, its swing is better than InAs/InGaAs channel devices. This may due to higher interface trap density at InAlAs/InAs interface than InGaAs/InAs.

The output characteristic of pure InGaAs, InAs/InGaAs and InGaAs/InAs/InGaAs channel MOSFET was compared in Figure 3.24 at V_g-V_{th} from 0 V to 2 V with a step of 0.5 V. Good saturation was achieved for InAs MOSFETs. The maximum drive current density at V_g-V_{th}=2V for InGaAs/InAs/InGaAs channel devices (L_g=20μm) is 131mA/mm, which is slightly higher than pure InGaAs channel devices (126mA/mm). The improvement of drive current at high gate voltage is not as significant as at low gate voltage. This may be due to the fact that at high electric field electrons spill over into InGaAs layer or the lower-mobility barrier layer.

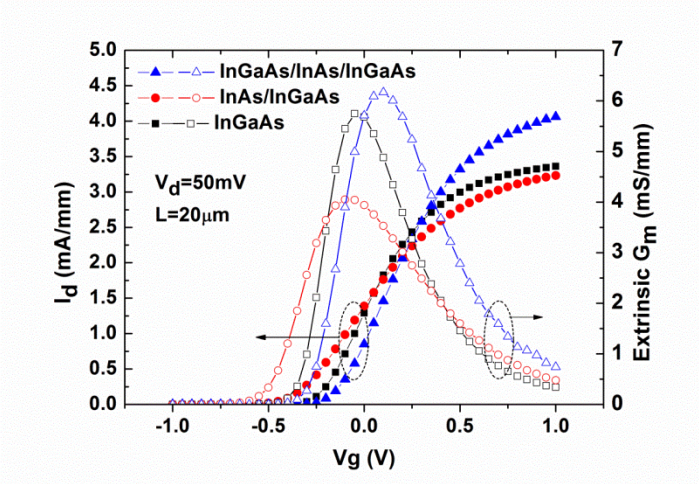


Figure 3.22. I_d-V_g and extrinsic transconductance G_m-V_g curves at V_d=50mV for InGaAs, InAs/InGaAs and InGaAs/InAs/InGaAs channel MOSFETs.

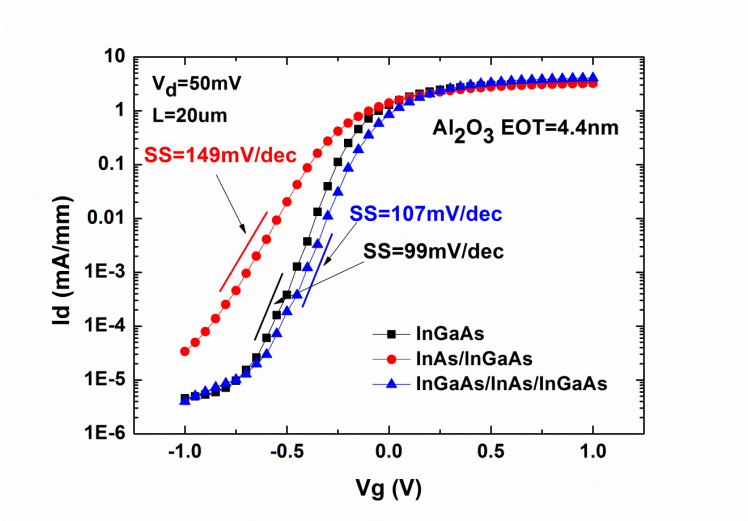


Figure 3.23. I_d-V_g subthreshold characteristics of InGaAs, InAs/InGaAs and InGaAs/InAs/InGaAs channel MOSFETs

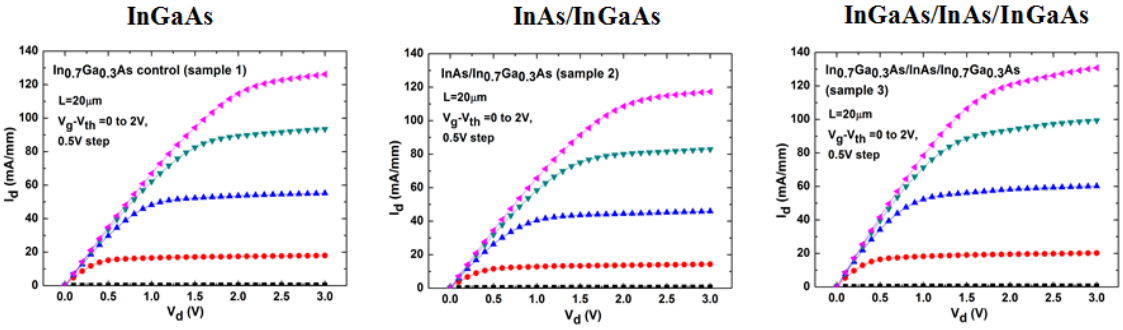


Figure 3.24. Output characteristics of pure InGaAs, InAs/InGaAs and InGaAs/InAs/InGaAs buried channel MOSFETs with gate length 20μm.

In order to reduce EOT, higher-k material HfO_2 has also been applied on InGaAs/InAs/InGaAs MOSFETs. The transfer characteristics of InGaAs/InAs/InGaAs MOSFETs with HfO_2 of EOT=1nm was shown in Figure 3.25. Compare to Al_2O_3,

although the EOT of HfO_2 is lower, devices with HfO_2 actually show higher SS and lower G_m. This is mainly due to the fact that HfO_2/InGaAs interface generates more interface traps than Al_2O_3/InGaAs.

The effective channel mobility of InAs/InGaAs channel, InGaAs/InAs/InGaAs channel and pure InGaAs channel buried channel MOSFETs have been measured using split-CV method and compared in Figure 3.26. The extracted channel mobility is consistent with I_d and G_m performance. The highest mobility of 6146cm^2/Vs has been achieved by InAs inserted in the middle of the channel layer of MOSFETs (at inversion charge density of 0.5×10^{12}/cm^2), which is ~115% peak mobility enhancement compared to "InAs on top" InAs/InGaAs channel devices. For pure InGaAs channel MOSFETs, the peak mobility is 5710cm^2/Vs (at inversion charge density of 0.5×10^{12}/cm^2). For the high field effective channel mobility (at inversion charge density of 3×10^{12}/cm^2), InAs inserted in the middle InGaAs/InAs/InGaAs channel devices show 37% increase over pure InGaAs channel devices. The effective channel mobility of InGaAs/InAs/InGaAs channel devices is 3370cm^2/Vs at inversion charge density of 3×10^{12}/cm^2. The results show that the effective channel mobility is sensitive to the location of InAs inserted layer. Split-CV measurement is illustrated in Figure 3.27. Temperature dependence has been studied on InGaAs/InAs/InGaAs MOSFETs. Transfer characteristics on temperature range from 77k to room temperature (RT) were plotted in Figure 3.28. Peak effective channel mobility increased from 6000cm^2/Vs at RT to 8000cm^2/Vs at 77k (see Figure 3.29).

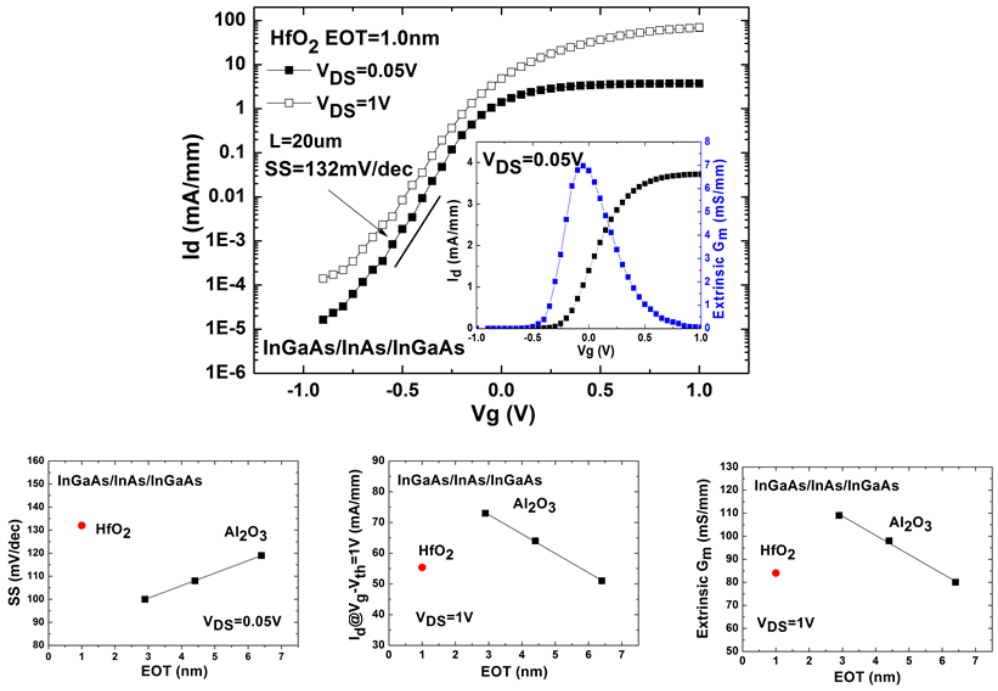


Figure 3.25. Transfer characteristics of InGaAs/InAl/InGaAs MOSFETs with HfO_2 and comparison of HfO_2 and Al_2O_3 on SS, Id and Gm vs. EOT.

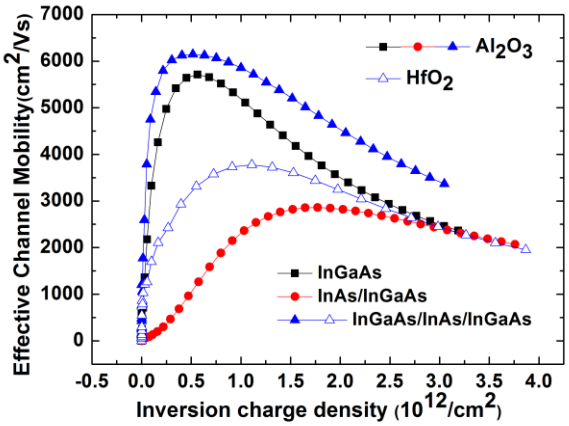


Figure 3.26. Effective channel mobility versus inversion charge density for InGaAs, InAs/InGaAs and InGaAs/InAs/InGaAs channel MOSFETs measured using split CV method.

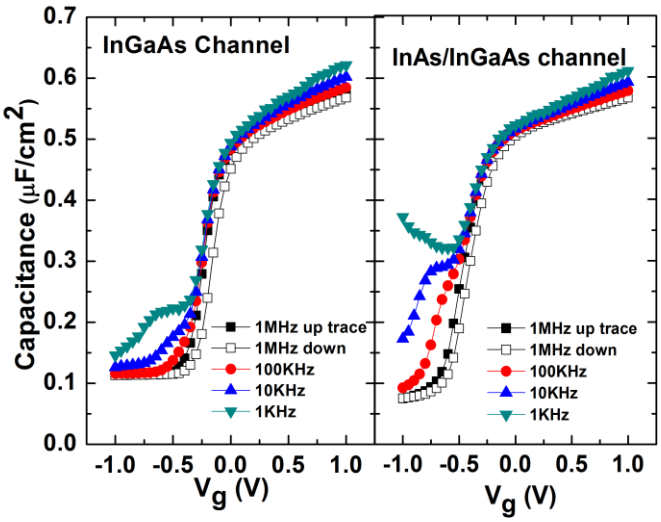


Figure 3.27. Multi-CV measurement on InGaAs channel and InAs/InGaAs channel MOSFETs with frequency range 1MHz to 1kHz.

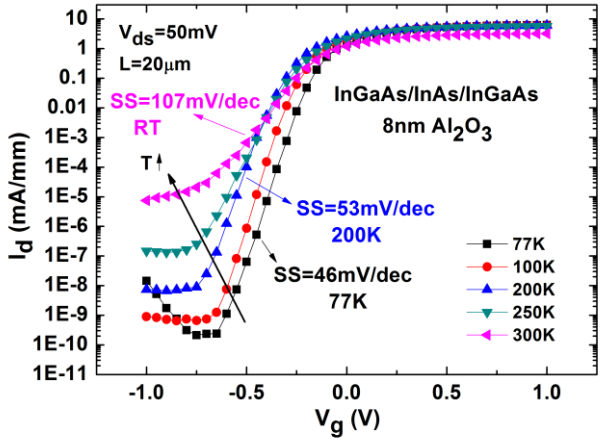


Figure 3.28. Low temperature measurement on transfer characteristics of InGaAs/InAs/InGaAs MOSFETs from 77k to RT

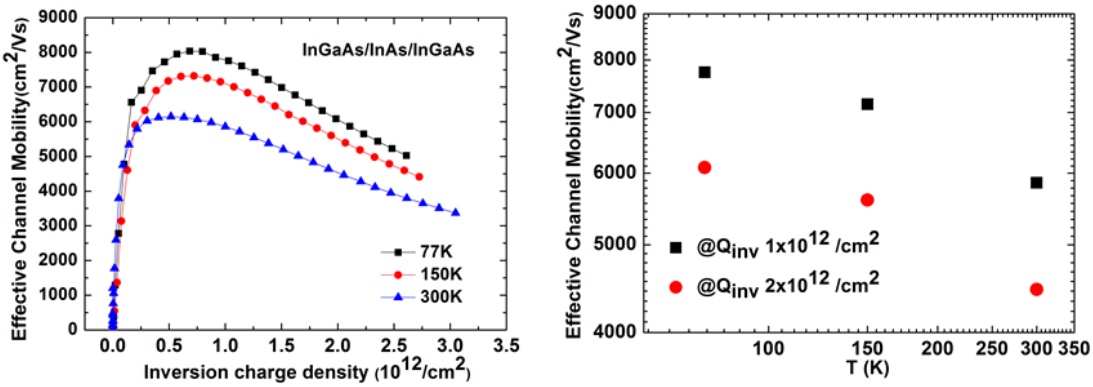


Figure 3.29. Low temperature measurement on effective channel mobility of InGaAs/InAs/InGaAs MOSFETs from 77k to RT.

The effects of inserting InAs layer into InGaAs channel MOSFETs have been investigated above. Good off-state property and saturation characteristics have been achieved by InAs buried channel MOSFETs. The on-off current ratio is around 1.2×10^4. The results also show that the location of InAs inserted layer plays an important role on device characteristics. Devices with InAs layer inserted in the middle of InGaAs channel exhibit improved drive current, transconductance and effective channel mobility. The peak channel mobility of 6146cm^2/Vs was achieved by InGaAs/InAs/InGaAs channel MOSFETs with ALD Al_2O_3 gate dielectrics.

Chapter 4: 3D InGaAs Gate-Wrap-Around FETs

Non-planner gate-wrap-around structures have been investigated and applied to III-V MOSFETs to enable further scaling for low power logic applications [5][78-81]. The gate-wrap-around device architecture is expected to provide the ultimate gate control over the channel, leading to a significantly improved off-state performance. However, InGaAs GWAFETs reported so far did not show benefits compared to the tri-gate or planar devices in terms of on/off current ratio, SS and DIBL, largely due to high leakage current and poor high-k/III-V interface quality. In this section, 3D GWAFETs with $In_{0.53}Ga_{0.47}As$ channel and atomic-layer-deposited (ALD) high-k dielectrics and metal gate that outperform tri-gate and planar devices will be presented. The high performance of 3D $In_{0.53}Ga_{0.47}As$ GWAFETs achieved in this work attribute to: 1) a novel device layout design with no undercut when removing the underlying InP layer. This results in more robust fin structures and a higher yield; 2) the optimized fin etching process by applying digital wet etch to achieve smooth sidewalls of the $In_{0.53}Ga_{0.47}As$ channels; 3) the high-quality Al_2O_3/TiN gate stack by novel plasma enhanced ALD process. Significant improvement on electrostatic control with DIBL 20mV/V and SS 80mV/dec was observed from InGaAs GWAFETs with W_{fin}=40nm and L_g=140nm. Details on structure design, fabrication process development and device performance will be discussed.

4.1 InGaAs GWAFETs Device Structure Design

Figure 4.1(a) illustrates the device structure of 3D $In_{0.53}Ga_{0.47}As$ GWAFET with the channel wrapped around by ALD Al_2O_3/TiN gate. Figure 4.1(b) shows the top view of fin structure without the gate stack. The layer structure, grown by MBE on the semi-insulating InP substrate, consists of 500 nm InP buffer layer, 50 nm $In_{0.53}Ga_{0.47}As$

channel layer, 1 nm InP barrier layer and 20 nm $In_{0.53}Ga_{0.47}As$ cap layer. All these layers were designed to be undoped, except for the top $In_{0.53}Ga_{0.47}As$ layer which is a heavily N-doped (Si 3e19cm^{-3}) layer intended for device source/drain (S/D). InP was chosen as the buffer layer to enable selective wet etch between $In_{0.53}Ga_{0.47}As$ and InP for releasing the $In_{0.53}Ga_{0.47}As$ fin structure. The addition of 1nm InP barrier layer performs as a wet etch stop layer at gate recess and it also separates the high-k dielectric/III-V interface from $In_{0.53}Ga_{0.47}As$ channel, therefore, the effective channel mobility is improved due to reduced carrier scattering. Figure 4.2 shows the layout of InGaAs GWAFETs. The reason to design fins in 45 degree aligned to S/D is to enable better control of fin releasing process. More details can be found in fabrication section.

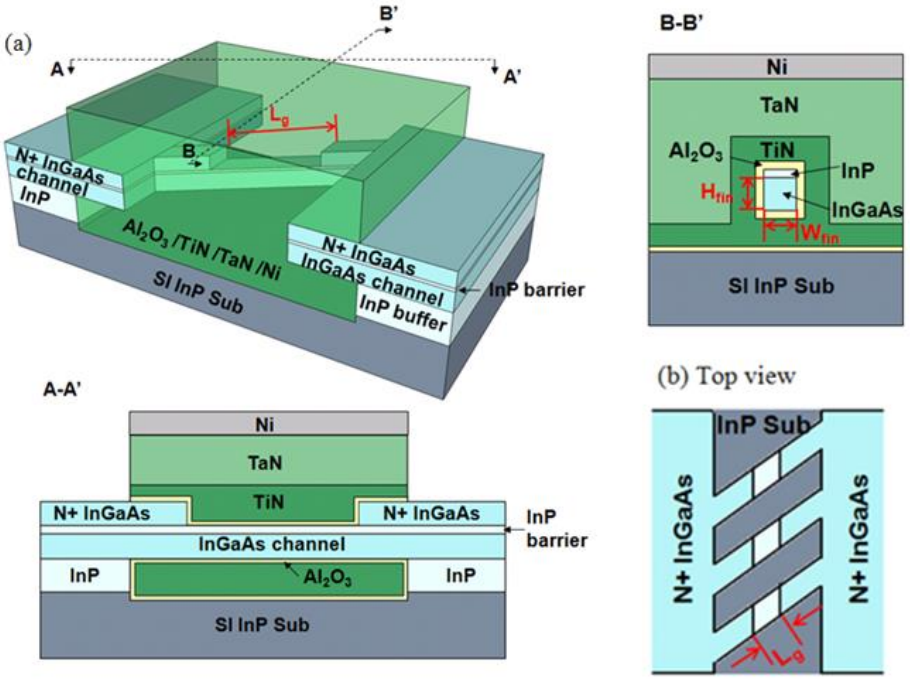


Figure 4.1 (a) Schematic structure of 3D $In_{0.53}Ga_{0.47}As$ GWAFETs with ALD Al_2O_3/TiN gate wrapped around. (b) Schematic top view of fin pattern after gate recess and fin construction.

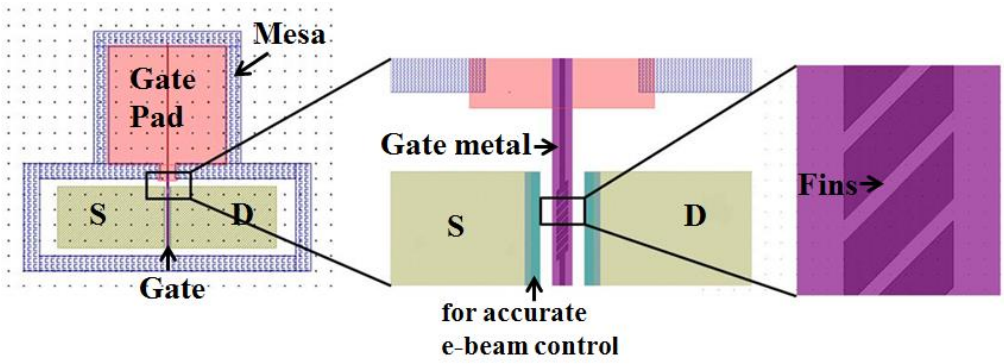


Figure 4.2 Layout of 3D InGaAs GWAFETs.

4.2 InGaAs GWAFETs Fabrication Process

The key fabrication steps are illustrated in figure 4.3. III-V substrate was first cleaned and protected by an ALD Al_2O_3 cap layer, followed by mesa isolation etching. Gate recess was done by using citric acid based wet etch to remove the n+ layer. Citric acid solution consists of citric acid: H_2O: H_2O_2 =60g: 60ml: 10ml. 30s dip was used to remove the 20 nm top n+ layer at gate region. Fins were then patterned by e-beam lithography using diluted ZEP520A. Fin dry etching was done by CH_4/H_2 inductively coupled plasma (ICP) using SiO_2 as hard mask. The fin patterning using SiO_2 as hard mask is presented in Figure 4.4. Fin dry etch is one of the key process of nanowire channel construction. Here the dry etch was done in cycles to reduce surface roughness and to better control etching rate. The dry etch is carried out by ICP etching with CH_2 2sccm H_2 9sccm at pressure 12mTorr. RF Power of 100W and ICP Power of 100W were applied. Each cycle of etching last 5min. 6 cycles were used to reach InP buffer layer. After dry etch, O_2 plasma descum was applied using ICP O_2 20sccm at pressure 20mTorr, RF Power 15W, ICP Power 1000W for 60s. A digital wet etch of $In_{0.53}Ga_{0.47}As$ was carried out by soaking samples in H_2O_2 and H_2SO_4 separately for a certain time to enable

fully chemical reaction [83]. Three cycles was used and ~5nm $In_{0.53}Ga_{0.47}As$ was removed on each side. This step is believed to reduce the surface roughness significantly after dry etch. InP buffer layer underneath channel was then removed by diluted HCl solution $HCl:H_2O=1:1$. InP etching is highly anisotropic. It etches very fast along [010] direction but stops along [110] direction. Fins are patterned in such a way that InP buffer underneath fins was etched in a fast rate without creating a large undercut in S/D area. If pattern the fins along [110] direction, InP underneath can hardly be removed. However, if pattern the fins along [010] direction, both InP underneath the fins and InP under source and drain region would be etched away quickly. This would leave a large undercut at source and drain. Thus here fins were designed to be 45 degree aligned with source and drain edge (see Figure 4.5). By using this approach, leakage current is dramatically reduced, fins are more robust and the device yield is improved. Figure 4.6 shows the InGaAs GWAFET channel structure released from the InP substrate with limited source and drain undercut. After fin construction, SiO_2 hard mask was removed by buffered oxide etch (BOE) and the sample was dipped in $(NH_4)_2S$ for surface passivation. 7nm ALD Al_2O_3 with equivalent oxide thickness of 3.6nm was deposited, followed by 60 nm plasma enhanced ALD TiN in the same chamber to wrap around the channel. TaN was then reactively sputtered on top to reduce the gate resistance. Gate was then defined by CF_4 RIE using Ni as the hard mask. The gate oxide at the source/drain was removed by BOE dip. Finally, S/D ohmic contact was formed by e-beam evaporation of Pd/Ge/Ti/Pd 200A/400A/100A/400A stack and rapid thermal annealing at 320℃ for 90s. S/D metal to gate distance is 1 μm. Devices with W_{fin} from 40 nm to 200 nm, the gate length of 140 nm and 280 nm, and various numbers of parallel channels were fabricated (see Figure 4.1 for L_g, W_{fin}, H_{fin} definition). Note that L_g and W_{fin} were measured by SEM inspection.

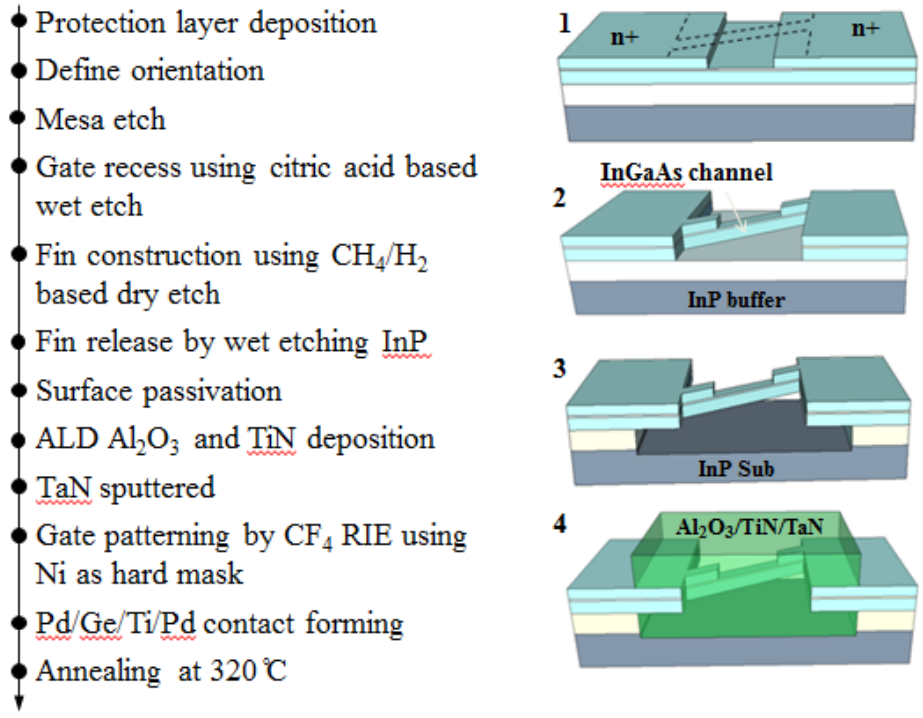


Figure 4.3 Key fabrication process steps of InGaAs GWAFETs.

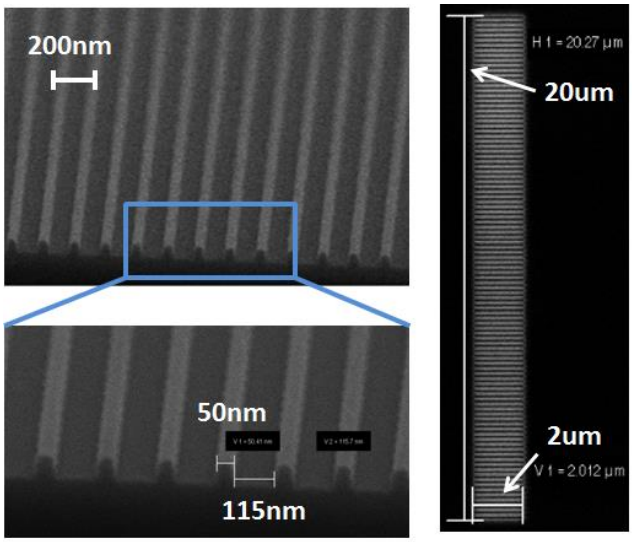


Figure 4.4 Test of fin patterning use SiO_2 as hard mask. This demonstrates the feasibility of using e-beam and SiO_2 hard mask to pattern fins across a large area.

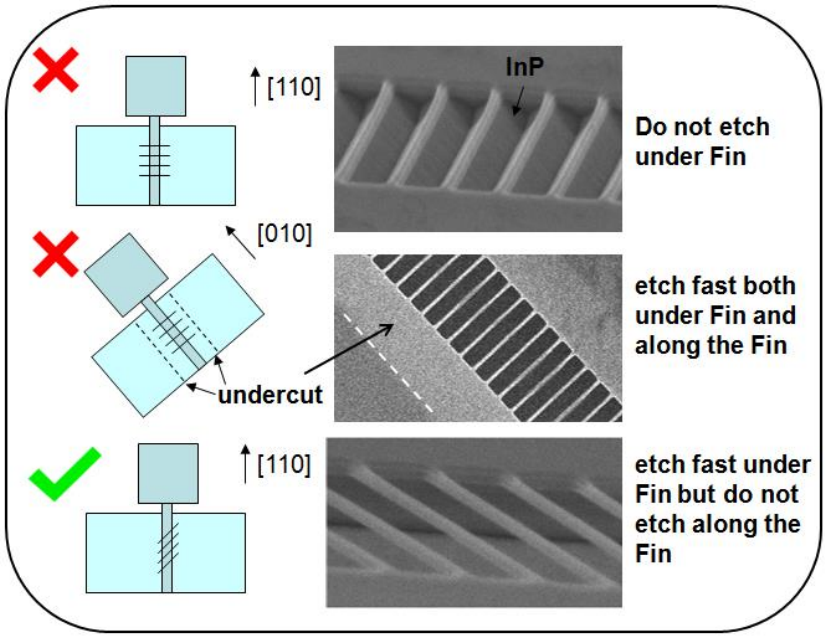


Figure 4.5 Improved $In_{0.53}Ga_{0.47}As$ GWAFETs device layout design to enable fast etching under the fin and limit undercut in source and drain region.

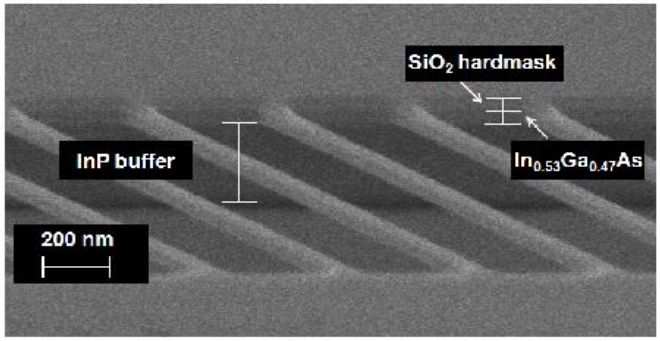


Figure 4.6 SEM image of $In_{0.53}Ga_{0.47}As$ channels released from InP substrate with limited InP undercut.

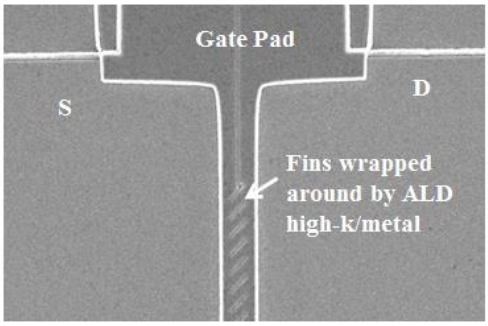


Figure 4.7 SEM of InGaAs GWAFETs with fins wrapped around by ALD of Al_2O_3 and TiN.

4.3 InGaAs GWAFETs Device Performances

The transfer characteristics of a typical $In_{0.53}Ga_{0.47}As$ GWAFET with W_{fin}=40 nm, Lg=140 nm, and 7 parallel channels are illustrated in Figure 4.8. Drive currents are normalized to the perimeter of InGaAs channels:

$$W_{tot} = (2W_{fin} + 2H_{fin}) \times (No.\,of\ channels) \quad (4.1)$$

The gate leakage is lower than 10^{-5} mA/mm. The device exhibits an on/off current ratio of around 4×10^4 at V_d=1 V. The off current is at $2*10^{-3}$ level at V_g=-0.2V and V_{ds}=0.5V. The off current is limited by the bulk leakage current since the device area is much larger than the fin area. The threshold voltage is extracted by the linear extrapolation of the maximum transconductance, which is to be 0.23 V for devices with L_g=140nm and W_{fin}=40nm. The undoped channel (with actual n type doping of 2e15 during MBE) should process a negative threshold voltage. Here the positive threshold voltage suggests a strong quantum confinement effect that raises the ground energy level. When increase the drain voltage from 0.5V to 1V, the drive current only increase around 22.5%. This indicates that external resistance is a strong factor that limits the drive current.

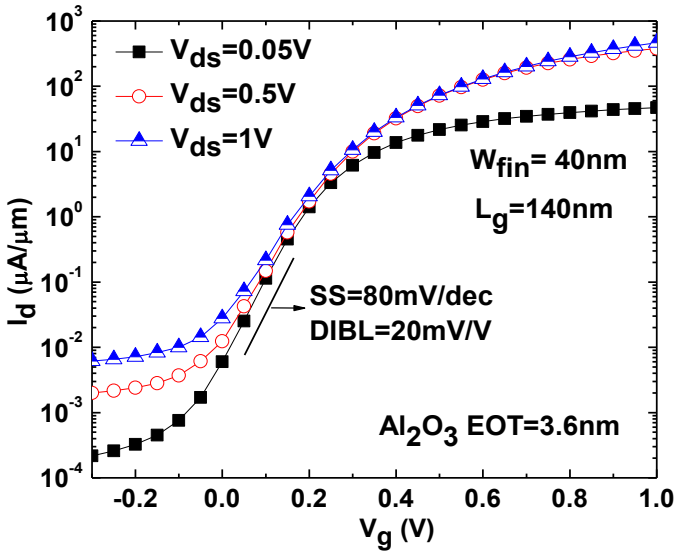


Figure 4.8 Transfer characteristics of InGaAs GWAFETs with L_g=140nn and W_{fin}=40nm.

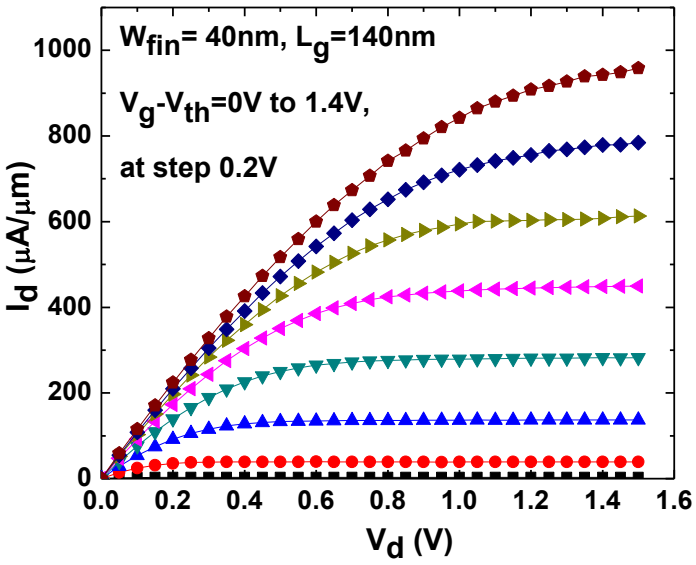


Figure 4.9 Output characteristics of GWAFETs with L_g=140nn and W_{fin}=40nm. Current is normalized to the perimeter of InGaAs channel.

The output characteristics of the same device is shown in Figure 4.9 and the device delivers I_d of ~613 μA/μm at V_d=1 V and V_g-V_{th}=1 V. The contact resistance was extracted by using gate length dependence to be ~930 ohm*μm. This high contact resistance may be due to the InP barrier layer at source and drain regions and the large S/D to gate distance. Contact fabrication process needs to be further optimized in order to improve the current drive characteristics of our devices.

Figure 4.10 compares the drive current and extrinsic transconductance (G_m) for devices with W_{fin} =40 nm, 60 nm and 100 nm. Higher current drive capacity and increased V_{th} were observed by narrowing down W_{fin} due to stronger quantum confinement effects. For narrower W_{fin} devices, carriers are confined further away from the high-k/III-V interface, thus scattering is reduced and the effective channel mobility is increased. Figure 4.11 shows the drain current of GWAFETs with W_{fin} =40 nm, 60 nm, 100 nm and 200nm. Reduced drain current overshoot from smaller W_{fin} devices indicates a better SCE control.

Figure 4.12 and Figure 4.13 show scaling metrics for $In_{0.53}Ga_{0.47}As$ GWAFET with various gate lengths and fin widths. Both drive current and transconductance per unit width increases with decreasing Wfin – a demonstration of the scalability of our device structures. Low SS values (80mV/dec) in Figure 4.14 suggest a high interface quality at $In_{0.53}Ga_{0.47}As$ channel sidewall and bottom surfaces. Al_2O_3/InP interface trap density (D_{it}) of around 1.5×10^{12}/eVcm^2 was extracted with the conductance method from planer devices. Figure 4.15 illustrates DIBL vs. W_{fin} for two gate lengths, where DIBL is measured at I_d = 1 μA/μm and V_d at 0.05 V and 0.5 V. DIBL reduces from 40 mV/V for W_{fin} = 200 nm to 20 mV/V for 40 nm devices, indicating a more effective gate coupling for narrower fin devices. SS and DIBL can be further reduced by gate dielectric scaling.

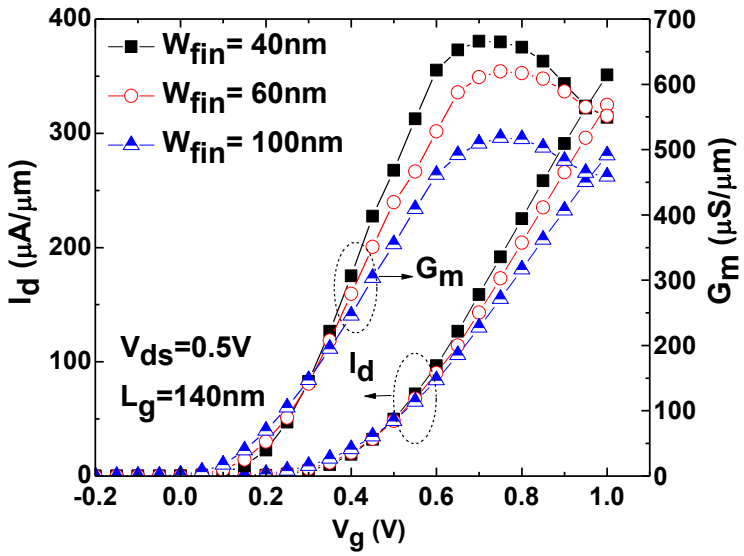


Figure 4.10 Comparison of drive current and extrinsic transconductance of InGaAs GWAFETs with W_{fin}=40nm, 60nm, 100nm at V_d=0.5V.

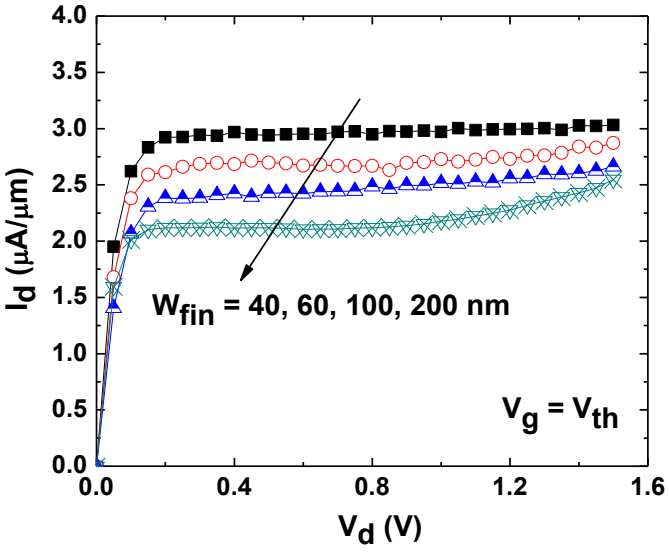


Figure 4.11 Drain current of InGaAs GWAFETs with W_{fin}=40nm to 200nm at V_g=V_{th}. Better short channel control was obtained by reducing W_{fin}.

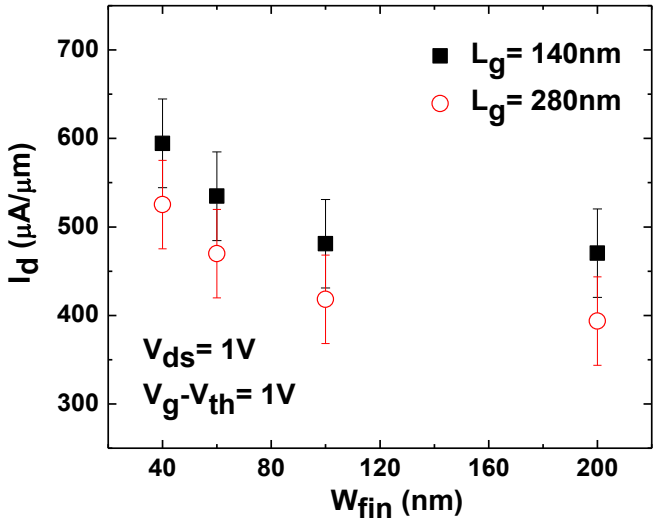


Figure 4.12 Drain current vs. W_{fin} of InGaAs GWAFETs with L_g=140nn and 280nm at V_{ds}=1V, V_g-V_{th}=1V.

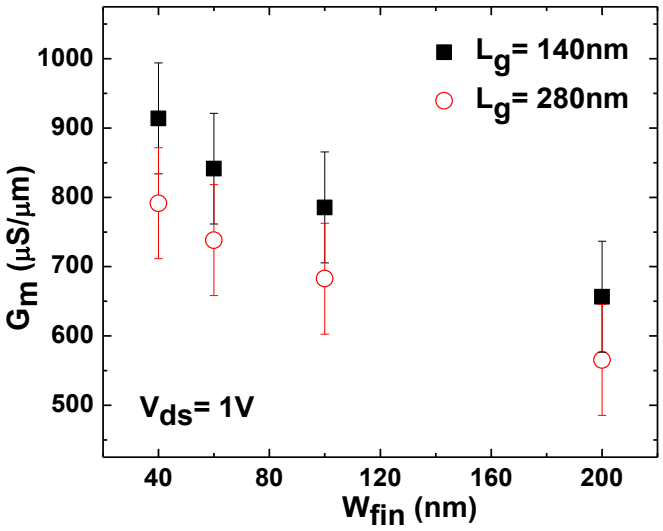


Figure 4.13 Extrinsic transconductance of InGaAs GWAFETs with L_g=140nn and 280nm at V_{ds}=1V.

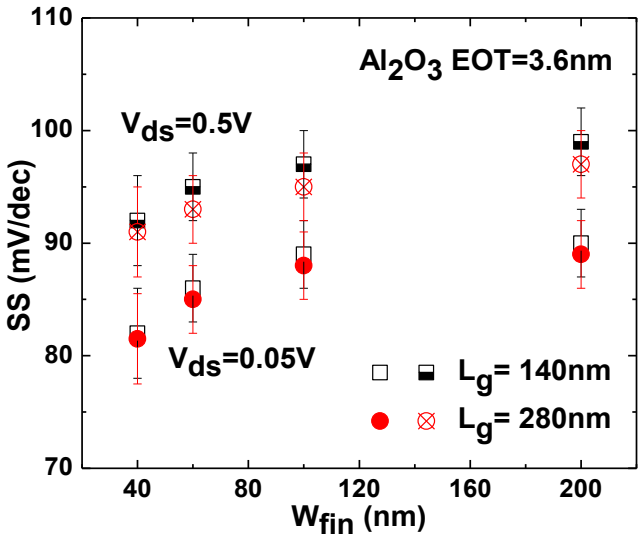


Figure 4.14 Subthreshold swing of GWAFETs at V_{ds}=0.05V and 0.5V with 7nm ALD Al_2O_3.

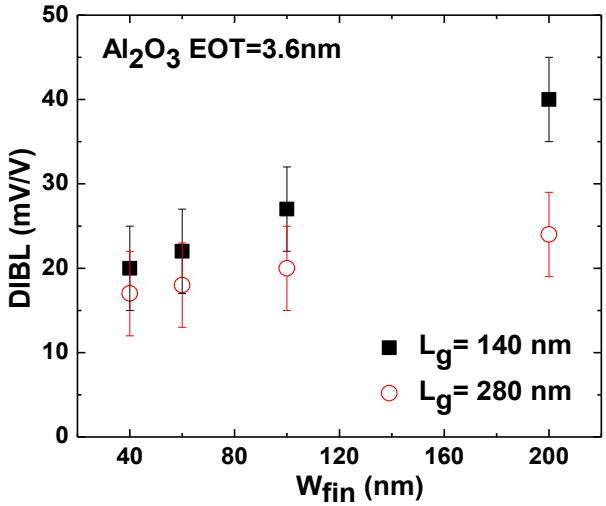


Figure 4.15 DIBL vs. W_{fin} of GWAFETs.

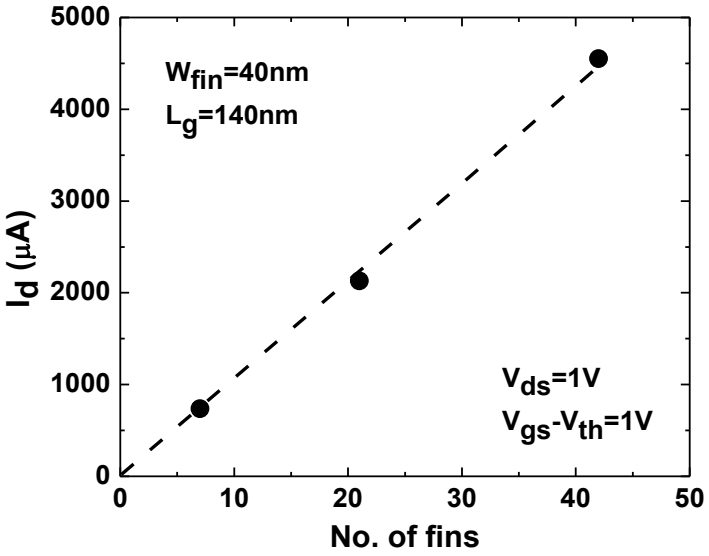


Figure 4.16 Drain current of $In_{0.53}Ga_{0.47}As$ GWAFETs with different number of fins.

Figure 4.16 shows the drain current of InGaAs GWAFETs with different number of fins. The drain current is linearly extrapolated to zero at zero number of fins. This indicates that there is no InP parasitic channel underneath the fins. It also shows a good scalability for higher integration density. The drive current for each fin is around 105 μA at V_g-V_{th}=1V and V_{ds}=1V.

4.4 SIMULATION OF INGAAS GWAFETS

The major components that degrade the current capacity of GWAFETs are believed to be 1) quantum confine effects of nanowire structure, 2) interface traps at high-k/III-V and 3) contact resistances at source and drain. In order to better understand each of these components, simulation on InGaAs GWAFETs has been carried out using Sentaurus device simulation. The nanowire structure with wrapped around high-k/metal

gate stack was adopted. Figure 4.16 presents InGaAs nanowire device structure and cross sectional view. $In_{0.53}Ga_{0.47}As$ channel is designed to be undoped, but here it is set to a low doping level of Si dopant at 2e15 cm^{-3} to simulate the MBE growth condition. Al_2O_3 of 7nm thickness, same as the experiment, was used here to wrap around the channel. TiN was applied as gate metal. Source and drain are configured by n+ InGaAs layer with Si doping level of 3e19 cm^{-3} and metal contact. Nanowire MOSFETs with diameter range from 10nm to 100nm were simulated.

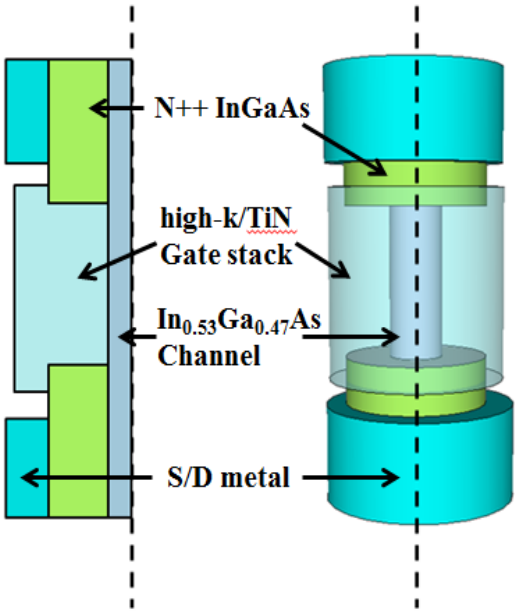


Figure 4.17 InGaAs nanowire structure and cross-sectional view for Sentuarus simulation.

Figure 4.17 illustrates the band structure and electron density distribution of InGaAs nanowire devices with diameter of 10nm, 20nm, 40nm and 100nm. It shows clearly that when the inversion layer is formed, for 100nm nanowire, electrons first accumulated at the surface. As the diameter of nanowire reduces, because of increased quantum confinement, the accumulation of electrons shifts to the center of nanowire.

When volume inversion occurs, the lower concentration of electrons in the channel would reduce the total current. Also, the distance between gate and central of electron distribution would increase and thus degrade the subthreshold swing characteristics. However, if take into consideration of surface roughness and the interface traps at dielectrics and channel, electrons shifting away from the surface could help reduce the scattering and thus enhance the transport. When reducing diameter of nanowire, III-Vs come into the volume inversion regime earlier because of their smaller effective mess compared to silicon, see Figure 4.18 for band structure and electron distribution of silicon nanowires with W_{fin} 10nm, 20nm, 40nm and 100nm.

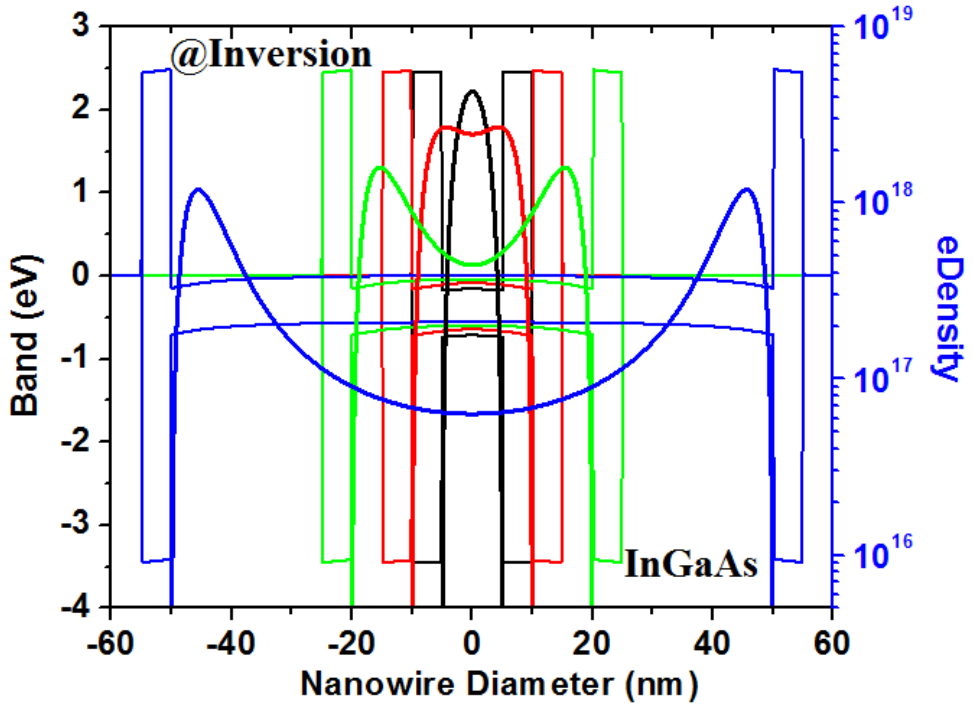


Figure 4.18 Band structure and electron density distribution of InGaAs nanowire devices with diameter of 10nm, 20nm, 40nm and 100nm.

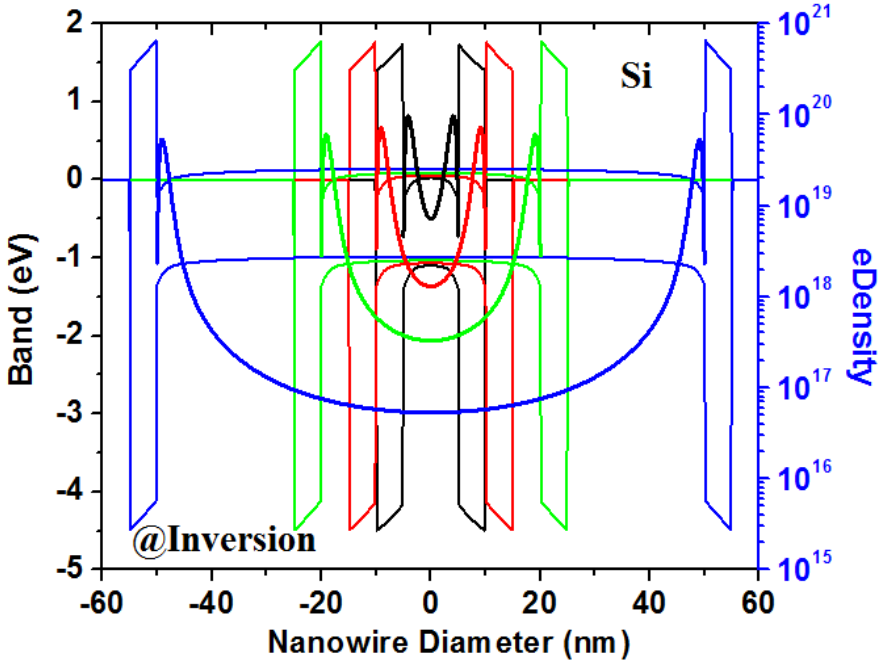


Figure 4.19 Band structure and electron density distribution of Si nanowire devices with diameter of 10nm, 20nm, 40nm and 100nm.

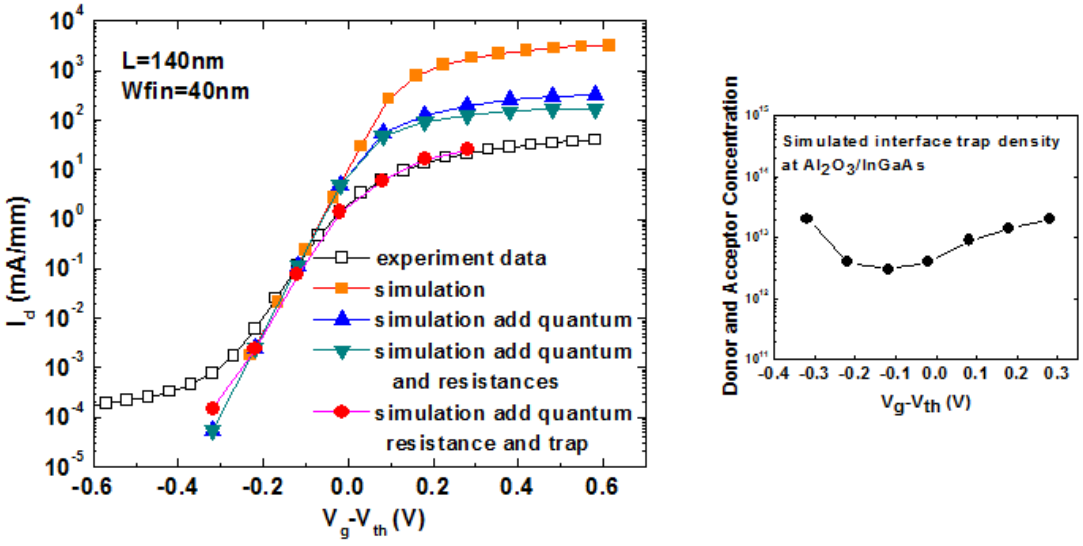
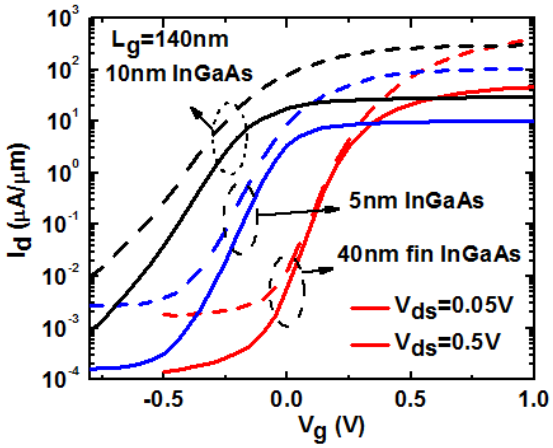


Figure 4.20 Experiment and simulation data of InGaAs nanowire to break down the current degradation mechanism. Interface trap density of high-k/InGaAs fitted in Sentuarus simulation was inserted.

In Figure 4.19, the degradation mechanism of drive current is broke down to several factors including quantum confinement effect, source and drain external resistance and interface trap scattering. Density gradient quantization model was used in Sentaurus to calculate the quantum effect on device performance. Simulation results suggest that by introducing quantum effect, the drive current drop accounts for 90% of the total difference between simulated data and experimental data. By adding the contact resistance of 1000ohm*um (extracted from experiment), the total current reduction is around 4.5%. The interface traps scattering accounts for the rest 5.5% current decrease. Interface trap density distribution as illustrated in Figure 4.19 with lowest D_{it} level of 3e12 $eV^{-1}cm^{-2}$ was applied to fit the simulation and experimental data.

4.5 COMPARISON OF INGAAS PLANAR MOSFETS AND 3D GWAFETS

The device performance of 3D InGaAs GWAFETs have been compared to planer InGaAs MOSFETs with similar substrate layer structures consisting of InGaAs channel, InP barrier layer and n+ InGaAs layer for source and drain. Figure 4.20 illustrates the I_d-V_g characteristics of InGaAs planer MOSFETs with 10nm and 5nm channel thickness and 3D InGaAs GWAFETs. DIBL and SS data are summarized and compared in the table aside. 10X drop on DIBL was observed from planar InGaAs MOSFETs at around 200mV/V to 20mV/V for 3D GWAFETs. By apply gate wrapped around structure SS also reduced 33%. Figure 4.21 shows the DIBL vs. gate length for 10nm, 5nm InGaAs channel planar MOSFETs and 3D GWAFETs with W_{fin} 200nm, 100nm, 60nm and 40nm. Better scalability was achieved by 3D GWAFETs compare to planar structure with lower DIBL, SS and higher drive current.



InGaAs FETs	DIBL (mV/V)	SS (mV/dec)
GWA W_{fin}=40nm	20	90
Planar 5nm Channel	121	100
Planar 10nm Channel	206	135

Figure 4.21 I_d-V_g characteristics of InGaAs planer MOSFETs with 10nm and 5nm channel thickness and 3D InGaAs GWAFETs. DIBL and SS comparison of planar and 3D InGaAs FETs.

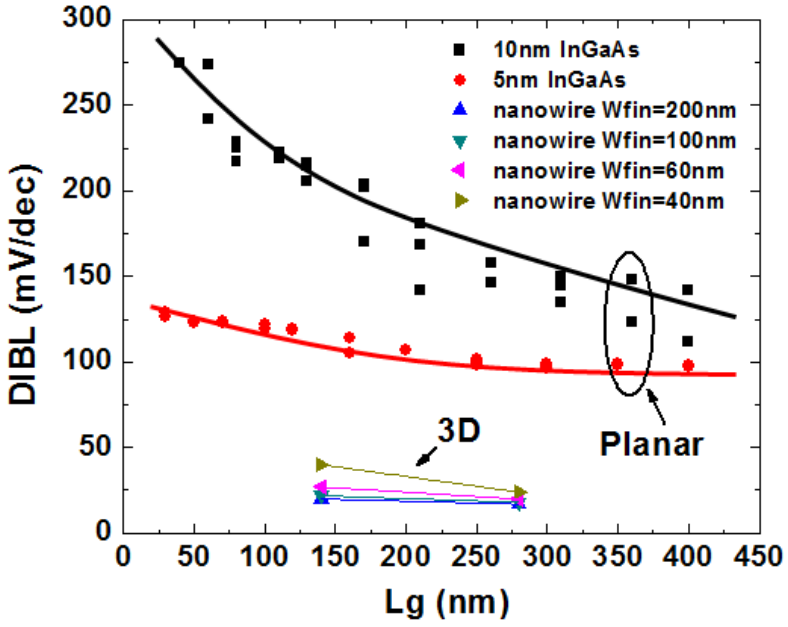


Figure 4.22 DIBL vs. gate length for 10nm, 5nm InGaAs channel planar MOSFETs and 3D InGaAs GWAFETs with W_{fin} 200nm, 100nm, 60nm and 40nm.

Table 4.1. Comparison of $In_{0.53}Ga_{0.47}As$ GWAFETs in this work with recently reported tri-gate, FinFET and planer QWFETs devices.

Device	Dielectric	L_g (nm)	W_{fin} (nm)	I_{on} (μA/μm)	I_{off} (nA/μm)	DIBL (mV/V)	SS (mV/dec)
$In_{0.53}Ga_{0.47}As$ GWAFET (This work)	7nm ALD Al_2O_3/ 1nm InP	140	40	600 (V_d=1V, V_g-V_{th}=1V)	6 (V_d=1V)	20	90 (V_d=0.5V)
$In_{0.53}Ga_{0.47}As$ GAAFET (Purdue, IEDM 2011)	10nm ALD Al_2O_3	50	30	450 (V_d=1V, V_g-V_{th}=1V)	4000 (V_d=1V)	210	150
		110	30	355 (V_d=1V, V_g-V_{th}=1V)	4000 (V_d=1V)	180	140
$In_{0.53}Ga_{0.47}As$ Tri-gate FET (Intel, IEDM 2011)	High-k Stack EOT=12Å	60	40	360 (V_d=0.5V, V_g=0.5V)	100 (V_d=0.5V)	65	100 (V_d=0.5V)
		120	30	--	--	35	85 (V_d=0.5V)
$In_{0.7}Ga_{0.3}As$ FinFET (NUS, EDL 2011)	19nm MOCVD HfAlO	130	220	220 (V_d=1V, V_g-V_{th}=1V)	10 (V_d=1.2V)	135	230
$In_{0.7}Ga_{0.3}As$ Planer QWFET (UT, EDL 2012)	6nm ALD Al_2O_3/ 1nm InP	40	--	476 (V_d=1V, V_g-V_{th}=1V)	100 (V_d=1V)	270	140
		130	--	430 (V_d=1V, V_g-V_{th}=1V)	100 (V_d=1V)	206	135

Table 4.1 summarizes device performance of $In_{0.53}Ga_{0.47}As$ GWAFETs in this work with other works on planner or non-planner III-V FETs, including previously reported $In_{0.53}Ga_{0.47}As$ QWFETs. The fact that higher drive current, lower I_{off}, reduced SS and DIBL are all achieved in our 3D InGaAs GWAFETs shows promise for using this device structure in future logic technologies.

In this chapter, high-performance 3D $In_{0.53}Ga_{0.47}As$ GWAFETs with high-k dielectrics and metal gate was demonstrated. Fabrication process of GWAFETs with fin

width down to 40nm has been developed using e-beam lithography. Low SS of 80 mV/dec, DIBL of 20 mV/V and high drive current of 600 mA/mm at V_d=1 V and V_g-V_{th}=1 V have been obtained by 3D InGaAs GWAFETs with gate length 140nm and fin width 40nm. $In_{0.53}Ga_{0.47}As$ GWAFETs have been demonstrated to exhibit improved performance over FinFETs and planar devices; and are promising candidates for future ultimately scaled MOSFET devices.

Chapter 5: InGaAs Tunneling FETs

As scaling come to the era of power consumption limitation, new device operation concept like inter-band tunneling attracts more and more interests. TFET has been considered as the alternative device structure because it gets away from the thermionic emission principle and can potentially achieve a less than 60mV/dec subthreshold swing [37][84-86]. With a smaller swing, threshold voltage can be reduced without the punishment of raising the off-state current thus lead to a lower power consumption. Si channel TFETs have been demonstrated to achieve subthreshold swing lower than 60 mV/dec. However, the on-current of these devices is low due to the large tunneling barrier. Since band to band tunneling strongly depends on the band gap of semiconductor, moving substrate material from silicon to germanium and lower band gap III-V materials could help improve device performance[87-89]. In this section, device structure and fabrication process of InGaAs with ALD gate dielectrics are discussed. $In_{0.7}Ga_{0.3}As$ TFETs have been fabricated using MBE tunneling junctions. Device performances of TFETs with tunneling junction formed between p++/i and p++/n+ were compared. The purpose of changing the un-doped region to n+ type is to reduce the tunneling distance and improve tunneling efficiency. High-k dielectrics of $LaAlO_3$ and ZrO_2 have been applied. $LaAlO_3$ provides an advantage of higher quality interface with InGaAs while ZrO_2 has higher k value which enable further EOT scaling. The effects of junction and gate stack design on drive current and subthreshold swing have been investigated and discussed. Device characteristics of Si TFETs, Ge TFETs and InGaAs TFETs have been compared at the end of this chapter.

5.1. INGAAS TFETS LAYER STRUCTURE DESIGN

The layer structure of InGaAs TFETs (Table 5.1) was grown by MBE on a 2 inch p++ InP substrate, followed by 300 nm heavily p-type doped $In_{0.53}Ga_{0.47}As$ layer. The tunneling junction was formed by a 6 nm p++ $In_{0.7}Ga_{0.3}As$ (Be 2×10^{19} /cm^3 doped) and 6 nm undoped $In_{0.7}Ga_{0.3}As$ heterostructure for sample 1, and 6 nm p++ $In_{0.7}Ga_{0.3}As$ (Be 2×10^{19} /cm^3 doped) and 6 nm n+ $In_{0.7}Ga_{0.3}As$ (Si 2×10^{18} /cm^3 doped) heterostructure for sample 2. The highly doped p++/n+ junction was designed to reduce the tunneling width and increase the tunneling electric field, thus improve the drive current and subthreshold swing.

Table 5.1. Layer structure of TFETs with p++/i and p++/n+ junction design

Layer	Type	Material	Mole Fraction	Thickness (A)	Dopant	CV Level
6	N++	In(x)GaAs	53	15000	Si	3.0e19
5	N	In(x)GaAs	53	300	Si	9.0e17
4	i	In(x)GaAs	53	1000		
3	i	In(x)GaAs	70	60		
2	P++	In(x)GaAs	70	60	Be	2.0e19
1	P++	In(x)GaAs	53	3000	Be	2.0e19
Sample 1						

Layer	Type	Material	Mole Fraction	Thickness (A)	Dopant	CV Level
6	N++	In(x)GaAs	53	15000	Si	3.0e19
5	N	In(x)GaAs	53	300	Si	9.0e17
4	i	In(x)GaAs	53	1000		
3	N+	In(x)GaAs	70	60	Si	2.0e18
2	P++	In(x)GaAs	70	60	Be	2.0e19
1	P++	In(x)GaAs	53	3000	Be	2.0e19
Sample 2						

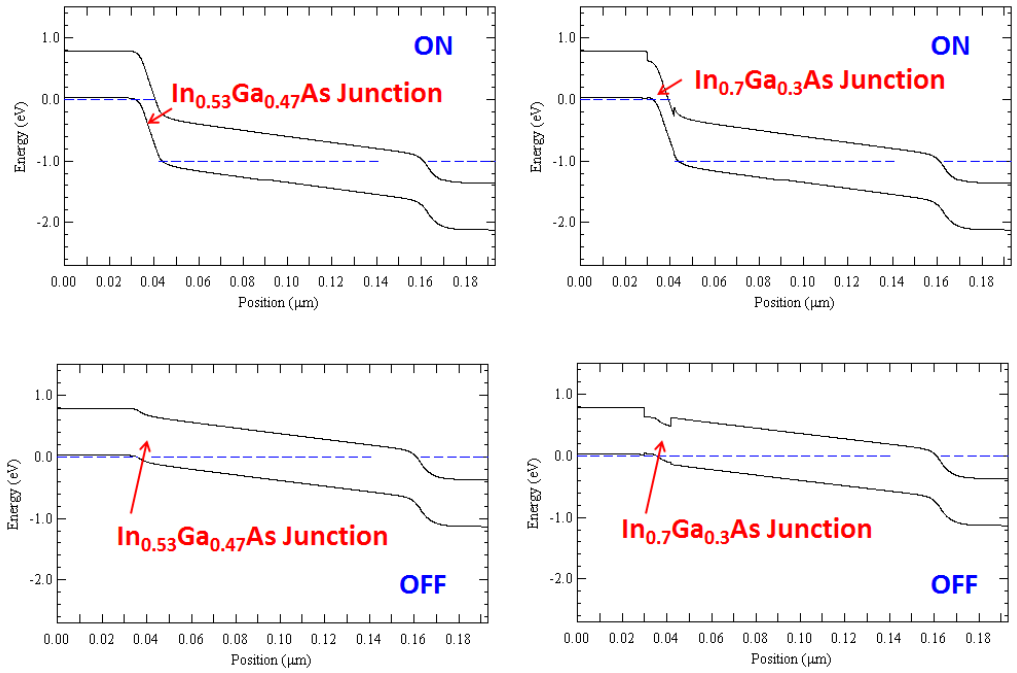


Figure 5.1. Band structure comparison of $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$

70% InGaAs is chosen here to further reduce the bandgap (Eg of $In_{0.53}Ga_{0.47}As$ is 0.74eV, E_g of $In_{0.7}Ga_{0.3}As$ is 0.58eV). However, the thickness of $In_{0.7}Ga_{0.3}As$ layer is limited by lattice mismatch between $In_{0.7}Ga_{0.3}As$ and InP. 12nm is the up-limit for MBE growth. The channel region is a 100 nm undoped $In_{0.53}Ga_{0.47}As$ layer. The top 150 nm n++ $In_{0.53}Ga_{0.47}As$ layer was designed for the drain contact. A 30 nm n- $In_{0.53}Ga_{0.47}As$ (Si 9×10^{17} /cm^3) was inserted between the n++ $In_{0.53}Ga_{0.47}As$ and the un-doped channel region to reduce the ambipolar conduction. That is to suppress transistor turning-on at negative gate voltage. Without this layer, n++ top layer is directly connected to the i type channel which will form another tunneling junction. This junction will turn on at negative gate voltage and positive drain voltage. Then the device can't be turned off.

5.2. InGaAs TFETs Fabrication Process

The schematic cross-sectional view of $In_{0.7}Ga_{0.3}As$ TFETs is shown in Figure 5.2. Top view of TFETs and cross-sectional SEM is inserted. These TEFTs were fabricated as follows: first the side wall was etched by citric acid based wet etch. The etch rate was optimized to reduce the surface roughness. The wet etch was controlled by time and it stop in the p++ $In_{0.53}Ga_{0.47}As$ layer. After diluted HF cleaning and ammonium sulfate passivation, high-k dielectric was deposited by ALD directly on InGaAs substrate as gate dielectrics. Gate electrode TaN was then deposited by sputtering. The drain contact was formed by e-beam evaporated AuGe/Ni/Au. The backside of the sample was deposited with Cr/Au as source contact. The wafer was then annealed in RTA at 300 °C in N_2 to form the source and drain contact.

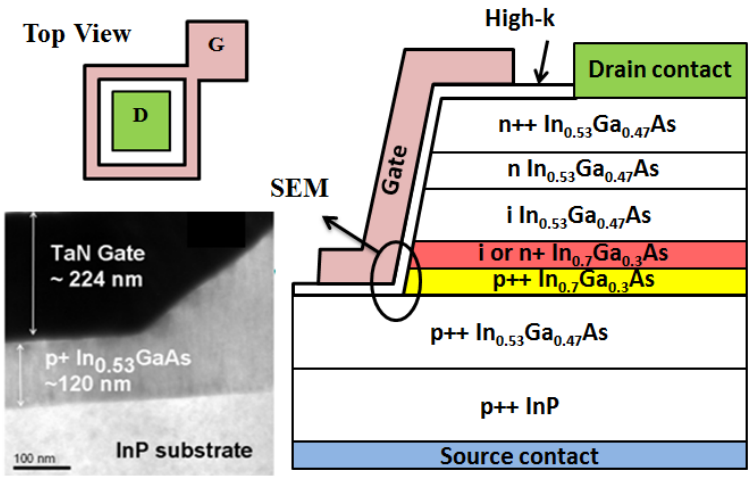


Figure 5.2. Schematic cross-sectional view of $In_{0.7}Ga_{0.3}As$ TFETs using p++/i or p++/n as tunneling junction and high-k $LaAlO_3$ or ZrO_2 gate dielectrics.

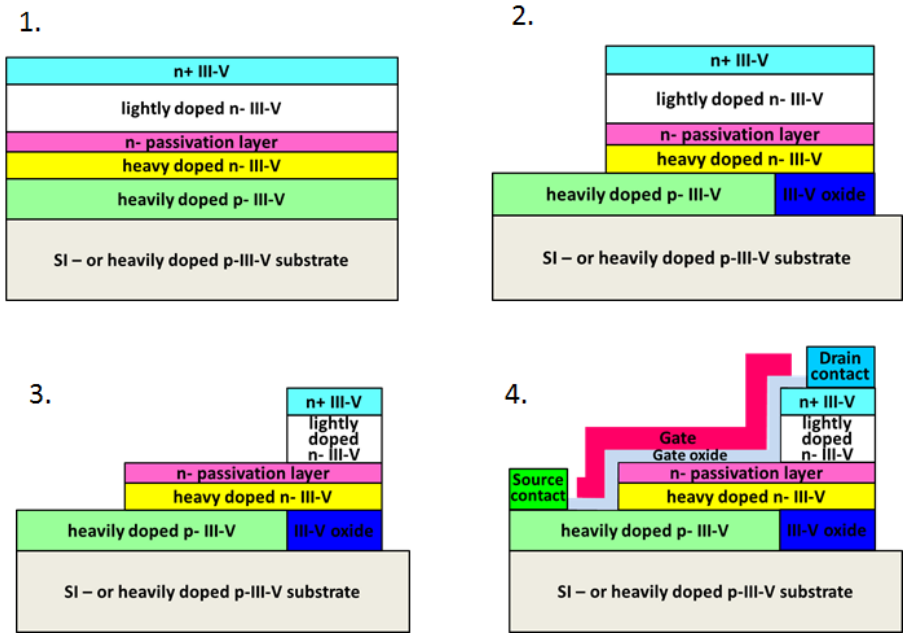


Figure 5.3. Device layer structure and key fabrication steps of lateral TFETs

Another type of TFETs with lateral structure has also been designed. The key fabrication steps were plotted in Figure 5.3. First the device isolation was done by wet etch down to substrate and partially oxidize the heavily doped p type layer to prevent drain voltage control of tunneling junction. Then wet etch controlled by time was applied to expose source and gate area. After deposition gate dielectric and metal, source and drain contact was defined at the last step. The advantage of lateral TFETs is that the tunneling area could be increased and thus drive current will be improved by a larger gate area. However, since the fabrication difficulty of the lateral TFETs, the vertical TFETs structure (Figure 5.2) was adopted in the following discussions.

5.3. JUNCTION DESIGN OF INGAAS TFETS

The design of tunneling junction is the key to ensure good device performance. Ideally, a sharp tunneling junction interface between p++ and i layers would be preferred. However, during the MBE growth, an intermixing layer would hardly be avoided. As the secondary ion mass spectrometry (SIMS) result indicated that diffusion length of Be into undoped layer is around 3nm to 5nm (Figure 5.4).

Figure 5.5 shows the device and band structure of TFETs with p++/n+ and p++/i junction. The subthreshold characteristics of TFETs with p++/i or p++/n+ tunneling junctions and $LaAlO_3$ (EOT~1.8nm) dielectric was illustrated in Figure 5.6. TFETs with p++/n+ tunneling junction exhibit lower subthreshold swing (96 mV/dec at V_{ds}=50 mV) than devices with p++/i tunneling (115 mV/dec at V_{ds}=50 mV). The output characteristics of TFETs with p++/i or p++/n+ tunneling junction is shown in Figure 5.7 measured at V_g-V_{th}=0 to 2 V, at the step of 0.5 V. The threshold voltage of TFETs with p++/i junction and p++/n+ junction is 0.18 V and 0.27 V respectively. Devices with p++/n+ junction exhibit 28% increase in drive current at V_g-V_{th}=2 V than devices with p++/i junction.

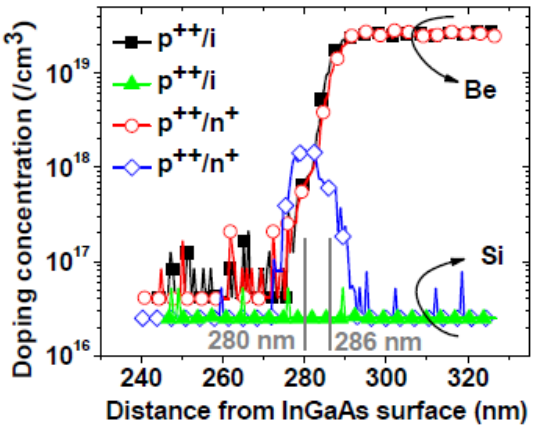


Figure 5.4. SIMS result of TFET layer structure with Be and Si doping.

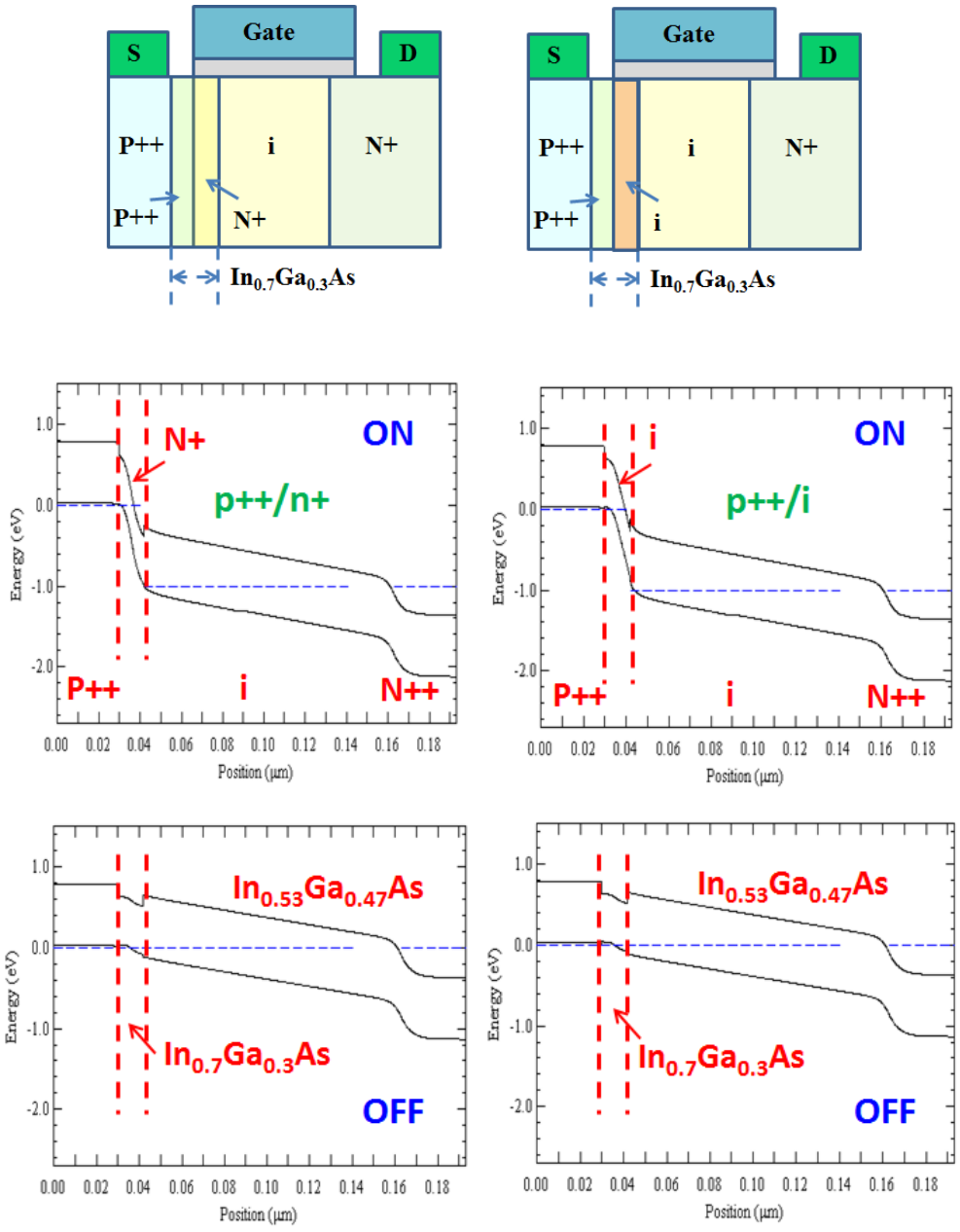


Figure 5.5. Device structure and band diagram of p++/n+ and p++/i junction.

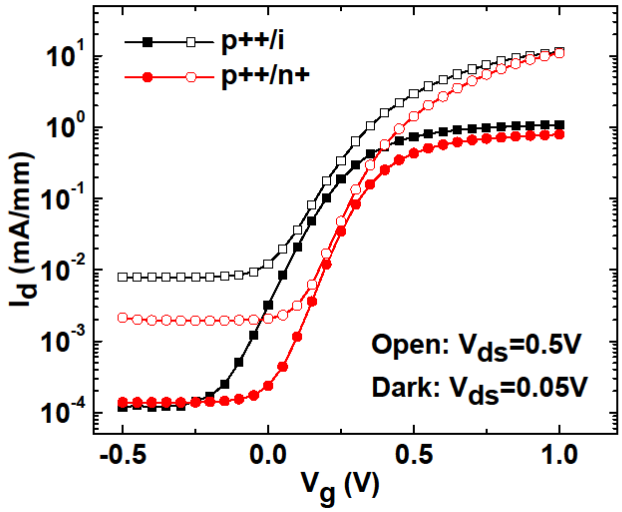


Figure 5.6. Subthreshold characteristics of $In_{0.7}Ga_{0.3}As$ TFETs with p++/i or p++/n+ tunneling junctions measured at V_{ds}=0.05 V and 0.5 V

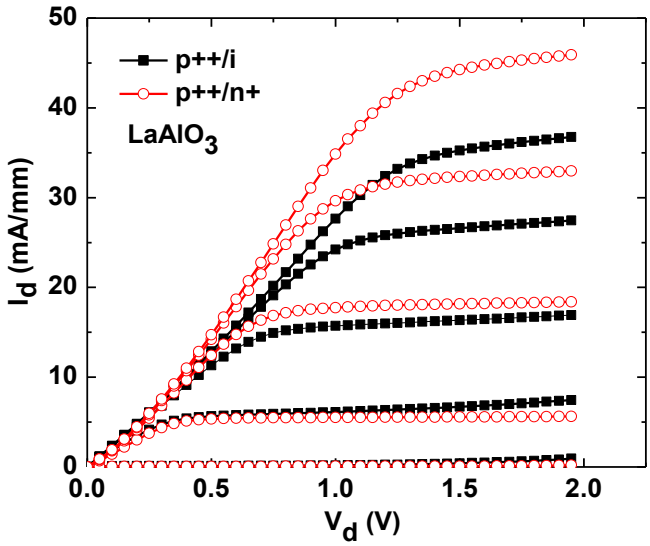


Figure 5.7. Output characteristics of $In_{0.7}Ga_{0.3}As$ TFETs with p++/i or p++/n+ tunneling junctions measured at V_g-V_{th}=0 V to 2 V at the step of 0.5 V.

The subthreshold swing values for these TFETs are still higher than 60 mV/dec (Figure 5.6). The main reasons for that is 1) the relatively poor III-V and high-k oxide interface. Interface traps at gate region would reduce the gate control over channel and thus degrade the subthreshold swing. 2) the tunneling junction at p++/i or p++/n+ is not ideal due to MBE growth. Dopant diffusion at annealing process would also degrade the subthreshold swing.

5.4. InGaAs TFETs with Scaled High-k Dielectrics

In order to further improve the subthreshold swing of TFETs, ZrO_2 has been applied as gate dielectric. The advantage of ZrO_2 is its higher k value (k=32 for ZrO_2 compared to k=13 for $LaAlO_3$). By applying the same physical thickness oxide layer, ZrO_2 can achieve smaller effective oxide thickness and thus enhance the gate control over channel. However, $LaAlO_3$ provides an advantage of higher quality interface with InGaAs (D_{it} of $LaAlO_3$/InGaAs ~1×10^{12} $eV^{-1}cm^{-2}$ vs. D_{it} of ZrO_2/InGaAs ~5×10^{12} $eV^{-1}cm^{-2}$). Interface trap density was measured by conductance methods. Device performance of $In_{0.7}Ga_{0.3}As$ TFETs with ZrO_2 oxide and p++/n+ tunneling junction is illustrated in Figure 5.8. The $In_{0.7}Ga_{0.3}As$ TFETs with ZrO_2 gate dielectric exhibit a subthreshold swing of 80 mV/dec at V_{ds}=0.05 V, and drive current of 44 mA/mm at V_g-V_{th}=2 V. The comparison of TFETs with 5 nm $LaAlO_3$ (EOT~1.8 nm) and 5 nm ZrO_2 (EOT~0.8 nm) gate dielectrics is shown in Figure 5.9. When the EOT of TFETs shrinks from 1.8nm for $LaAlO_3$ to 0.8 nm for ZrO_2, the minimum SS dropped from 96mV/dec to 80mV/dec. InGaAs TFETs with ZrO_2 gate oxide exhibit smaller swing than $LaAlO_3$ due to a better gate coupling.

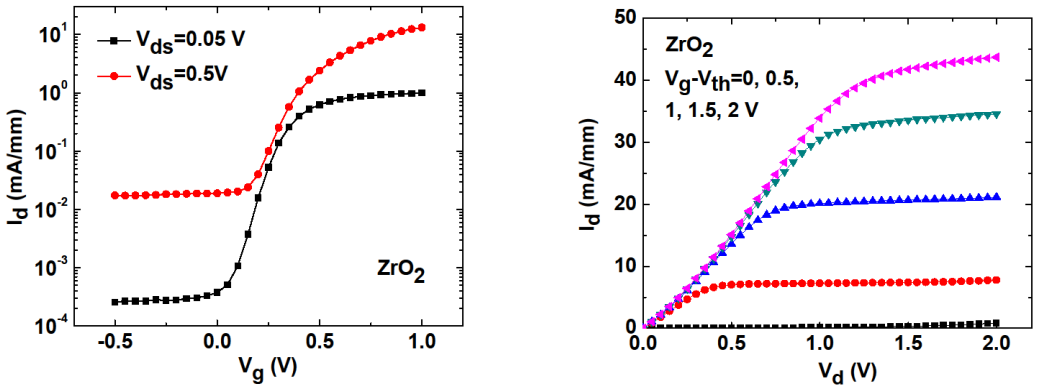


Figure 5.8. a) Subthreshold characteristics of $In_{0.7}Ga_{0.3}As$ TFETs with ZrO_2 and p++/n+ tunneling junctions measured at V_{ds}=0.05 V and 0.5 V. b) the output characteristics of $In_{0.7}Ga_{0.3}As$ TFETs with ZrO_2 and p++/n+ tunneling junctions measured at V_g-V_{th}=0 V to 2 V at the step of 0.5 V.

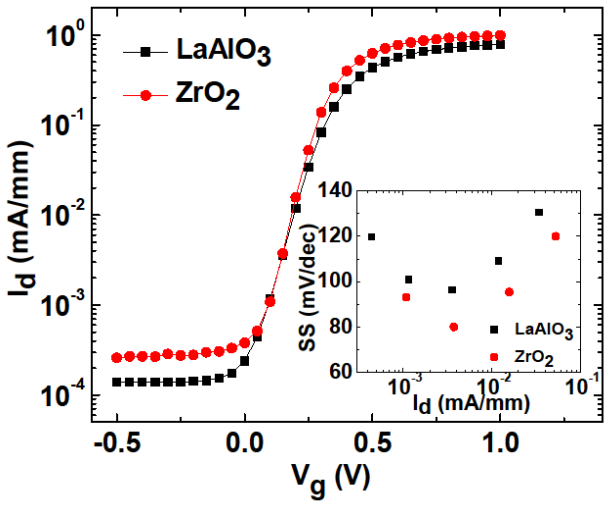


Figure 5.9. Subthreshold characteristics of $In_{0.7}Ga_{0.3}As$ TFETs with ZrO_2 or $LaAlO_3$ gate dielectrics on p++/n+ tunneling junction. Subthreshold swing vs. I_d for both devices are inserted.

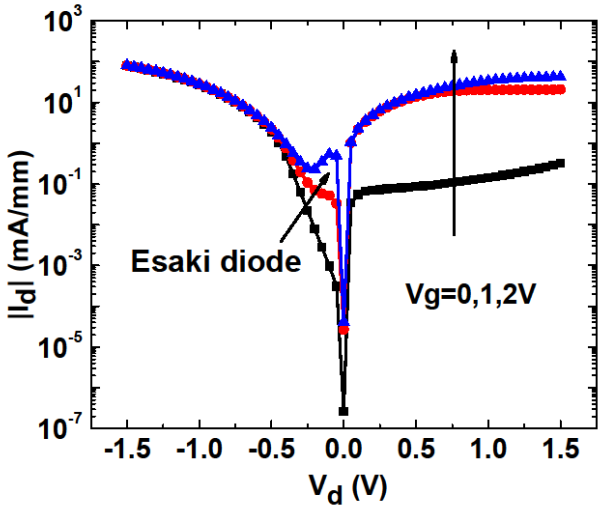


Figure 5.10. Log-scale $|I_d|$~V_d characteristics measured at V_g=0, 1, 2 V. Esaki diode behavior at forward diode bias (negative drain voltage).

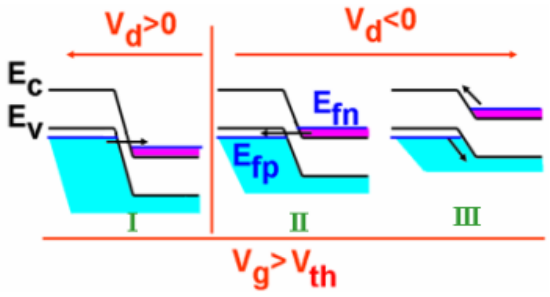


Figure 5.11. The Esaki diode mechanism [40].

Figure 5.10 shows the log-scale $|I_d|$ versus V_{ds} measured at V_g=0, 1, 2 V. Esaki diode behavior [40] was observed at V_{gs}>V_{th} and forward diode bias V_{ds}< 0 V. The negative differential resistance region is result from the electron tunneling from the n-side conduction band to the p-side valence band when a negative V_{ds} (forward bias on diode) is applied. This Esaki diode behavior demonstrates the band-to-band tunneling mechanism (Figure 5.11). Table 5.2 summarized the key device performance of Si, Ge and InGaAs TFETs.

Table 5.2. Comparison of Si, Ge, $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ TFETs key device performances

Channel Material	V_{GS} (V)	V_{th} (V)	V_{DS} (V)	SS (mV/dec)	I_{on} (mA/mm)	I_{on}/I_{off}
$In_{0.7}Ga_{0.3}As$	2	0.18	1	80	44	$>10^4$
$In_{0.53}Ga_{0.47}As$ [S. Mookerjea, IEDM 2009]	2.5	~0	0.75	150~290	20	$>10^3$
Ge [T. Krishnamohan, IEDM 2008]	4	~0.25	1	50~60	10	10^6
Ge [F Mayer, IEDM 2008]	2		0.8	>400	4	$>10^2$
Si [W Choi, IEDM 2007]	1	0.12	1	52.8	12	10^4
Si [F Mayer, IEDM 2008]	3	~0	0.8	42-200	0.02	10^5

In this chapter, the fabrication process and device performance of $In_{0.7}Ga_{0.3}As$ TFETs with high-k gate dielectrics were investigated. In order to improve the subthreshold swing characteristics, highly doped tunneling junction p++/n+ was applied. $In_{0.7}Ga_{0.3}As$ TFETs with p++/n+ tunneling junction exhibit improved subthreshold swing and drive current than TFETs with p++/i tunneling junction. Improvement of subthreshold characteristics was also achieved by reducing gate dielectric. The $In_{0.7}Ga_{0.3}As$ TFETs with ZrO_2 (EOT~0.8nm) gate dielectric exhibit a subthreshold swing of 80 mV/dec at V_{ds}=0.05 V and a drive current of 44mV/dec at V_{gs}=2V. The device performance of TFETs can be further improved by 1) sharper tunneling junction and 2) better quality high-k/III substrate interface.

Chapter 6: Conclusion and Future Work

6.1. CONCLUSION

At the time of finishing up this dissertation, Intel's 22nm multi-gated MOSFETs on silicon has already been launched for around a year. 14nm technology node is also approaching the end of development phase with FinFET structure still on silicon. Research is pushing into 7nm and 5nm technology node with new concepts on material and structure – III-V high mobility material, 2D material, bi-layer graphene, nanowire, TFETs, spin devices. This research work looks at III-V materials in explicit for MOSFET application, aims at advancing their device performance through novel device structures and better fabrication techniques.

First, interface and bulk properties of high-k dielectrics deposited using ALD on InGaAs substrate were studied. Among the high-k dielectrics, ZrO_2 shows the highest scalability while Al_2O_3 exhibits the best interface quality on InGaAs with the lowest D_{it}. Surface channel InGaAs MOSFETs were then investigated. Peak mobility of 1600cm^2/Vs was achieved using $In_{0.53}Ga_{0.47}As$ channel MOSFETs with Al_2O_3. $In_{0.53}Ga_{0.47}As$ MOSFETs were found to exhibit better device performance than $In_{0.7}Ga_{0.3}As$ MOSFETs including higher transconductance, higher mobility and lower subthreshold swing. This is due to a better interface at $In_{0.53}Ga_{0.47}As$/oxide confirmed by D_{it} and CV frequency dispersion measurement.

Second, buried channel devices with a thin barrier layer between channel and dielectrics were designed and demonstrated to exhibit higher mobility than surface channel MOSFETs. Compared to devices without barrier, by adding 1nm InP barrier layer, the peak mobility and high electrical field mobility are increased by 65% and 51% respectively. The highest effective channel mobility around 5700cm^2/Vs was achieved by InP/InAlAs double barrier devices at inversion charge density of 0.5×10^{12}/cm^2. Improved

mobility for buried channel structure is due to reduced scattering from high-k/III-V interface. While the buried channel MOSFET structure improved the on-state performance significantly, the tradeoff is that it degrades the short channel effect control. $In_{0.7}Ga_{0.3}As$ channel devices with barrier layer exhibit much higher drive current and transconductance (for L_g=40nm InP/InAlAs double barrier device, G_m=570mS/mm at V_{ds}=1V) than devices without barrier layer (for L_g=40nm, G_m=330mS/mm at V_{ds}=1V), while subthreshold swing and DIBL are lower for devices without barrier layer (for Lg=40nm device, SS=103mV/dec, DIBL=131mV/V). To improve the short channel effect control for buried channel devices, devices with thinner channel were studied. The 5 nm $In_{0.7}Ga_{0.3}As$ channel (L_g= 40 nm) devices exhibit a reduced SS of around 100 mV/dec and DIBL of 128 mV/V compared to 10 nm $In_{0.7}Ga_{0.3}As$ channel devices (SS ~140 mV/dec, DIBL ~275 mV/V). However, the drawback for thinner channel devices is that the effective channel mobility also decreases. At inversion charge density of $3\times10^{12}/cm^2$, 10 nm $In_{0.7}Ga_{0.3}As$ channel devices exhibit mobility of 1860 cm^2/Vs vs. mobility of 1460 cm^2/Vs for 5 nm $In_{0.7}Ga_{0.3}As$ channel devices.

Third, to enable further scaling for III-V devices, 3D GWAFETs were created. Fabrication process of $In_{0.53}Ga_{0.47}As$ GWAFETs with fin width down to 40nm has been developed. Low SS of 80 mV/dec, DIBL of 20 mV/V and high drive current of 600 mA/mm at V_d=1 V and V_g-V_{th}=1 V have been obtained by 3D InGaAs GWAFETs with gate length 140nm and fin width 40nm. 3D $In_{0.53}Ga_{0.47}As$ GWAFETs have been demonstrated to exhibit improved performance over FinFETs and planar devices.

Last, $In_{0.7}Ga_{0.3}As$ TFETs for low power application were demonstrated. Highly doped tunneling junction p++/n+ was applied to reduce tunneling width and thus improve subthreshold swing and drive current compares to TFETs with p++/i tunneling junction. Improvement of subthreshold characteristics was also achieved by reducing gate

dielectric thickness. The $In_{0.7}Ga_{0.3}As$ TFETs with ZrO_2 (EOT~0.8nm) gate dielectric exhibit a subthreshold swing of 80 mV/dec at V_{ds}=0.05 V and a drive current of 44mV/dec at V_{gs}=2V.

6.2. FUTURE WORK

6.2.1. Lateral InGaAs 3D GWAFETs with Higher Integration Density

The 3D GWAFETs developed in this work process only one layer of InGaAs channel. It can be easily extended to multi-channel layer structure with InGaAs/InP/InGaAs/InP… layers. By stacking up these nanowire channels, the current drive capacity under certain area can be largely improved. The proposed device structure design is shown in Figure 6.1. The channel layer InGaAs is undoped. Thickness can vary to create different fin sizes. InP layers are designed to be heavily doped to reduce source and drain external resistances. In the fabrication process, at fin dry etch step, InP buffer layer should be reached. In this way, during fin release wet etching, all InP layers can be removed at the same time. Distance between InGaAs channel layers should be large enough to have low resistance metal gate wrapped around channel. At source and drain, contact holes are need for metal to contact each of the n++ InP layer to reduce parasitic resistances.

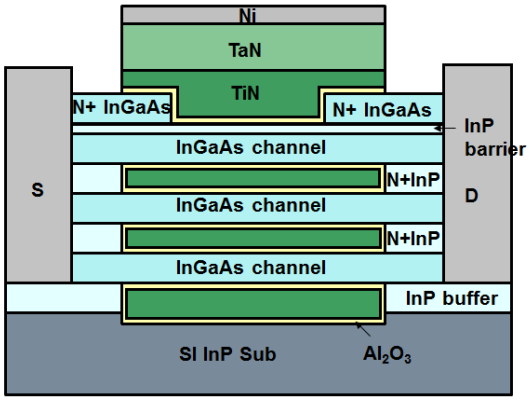


Figure 6.1. The proposed device structure design for lateral InGaAs GWAFETs with multiple channel layers.

6.2.2. InGaAs 3D GWAFETs with Reduced Nanowire Size

Smaller size nanowire channels are desired to study the quantum effects related issue. Nanowire FETs are designed for sub 10nm technology node, at such small size, electron density distribution and transport properties will change. Smaller size InGaAs nanowire channel can be achieved by slightly changing the process flow. In previous study, during fin releasing step, a digital wet etching process was carried out to smooth the surface of fins. Three cycles were used to remove around 5nm on each side of the fins. More cycles of digital wet etch can be applied to reduce fin width. Since the wet etch is self-limiting. Thickness control can be done precisely under nanometer level. Fins along different direction should be investigated. In strong quantum confinement, electrons tend to move into higher valley where the effective m* change and mobility is no longer symmetric. By designing substrate and channel orientations, device structure with high mobility (light effective mess) along transport direction and high density of states (heavy effective mess) perpetual to transport direction might be able to achieve.

6.2.3. Vertical 3D GWAFETs

Vertical nanowire GWAFETs can be fabricated by applying the novel nano-sphere lithography technique. This low cost, self-assembled fabrication process can create high density vertical nano-pillar structures. SiO_2 is deposited on III-V surface to be used as hard mask for pillar etching. Nano spheres are then applied to cover the surface using Langmuir-Blodgett methods. The size of the nano-sphere can be controlled by oxygen plasma. Nano pillars on III-V substrate can be formed using dry etching process same as used in lateral 3D GWAFETs. Key process steps for vertical 3D GWAFETs are shown in Figure 6.2.

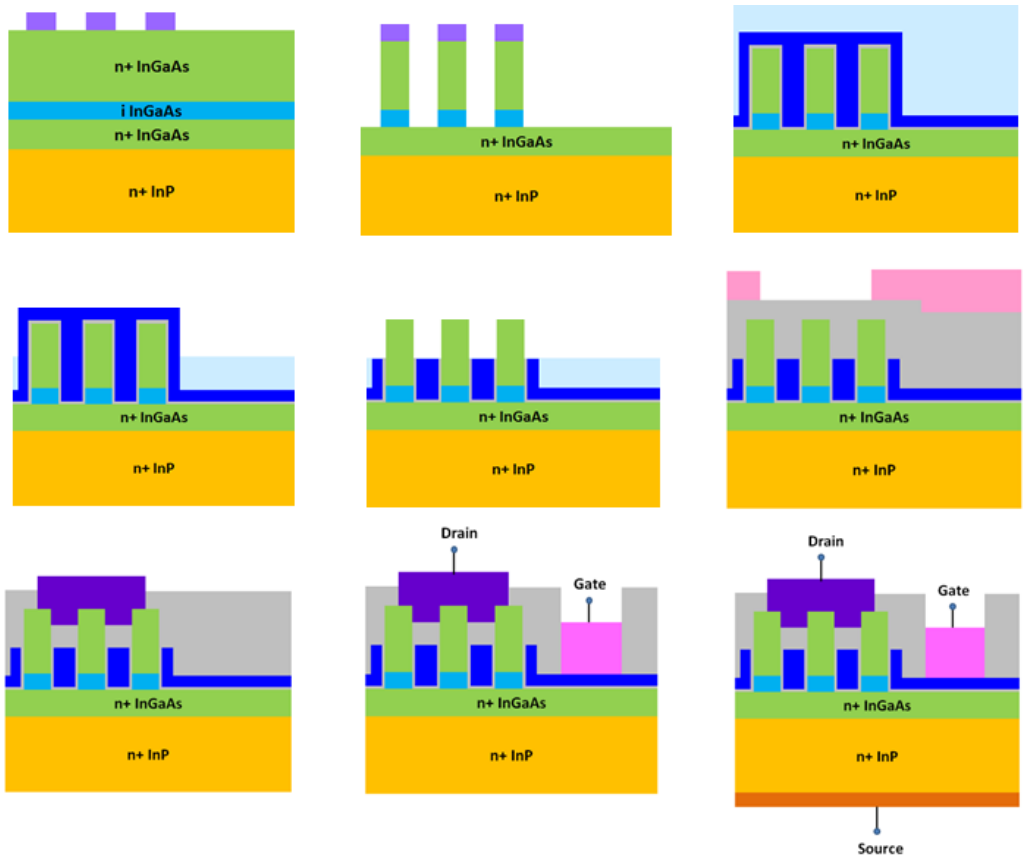


Figure 6.2. Key process flow for vertical 3D GWAFETs

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